FIG. 1

PRIOR ART

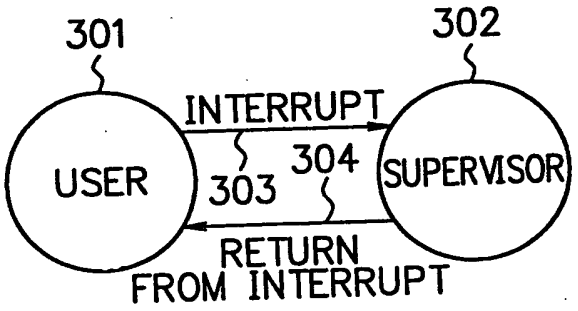
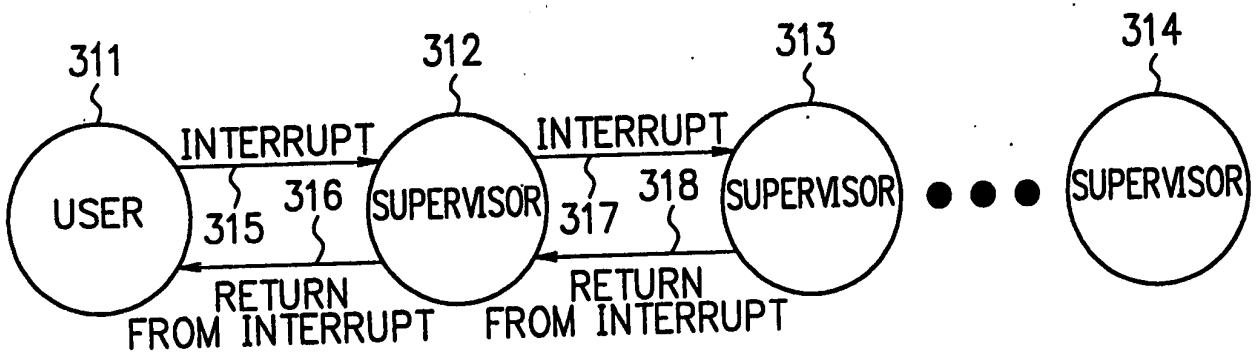
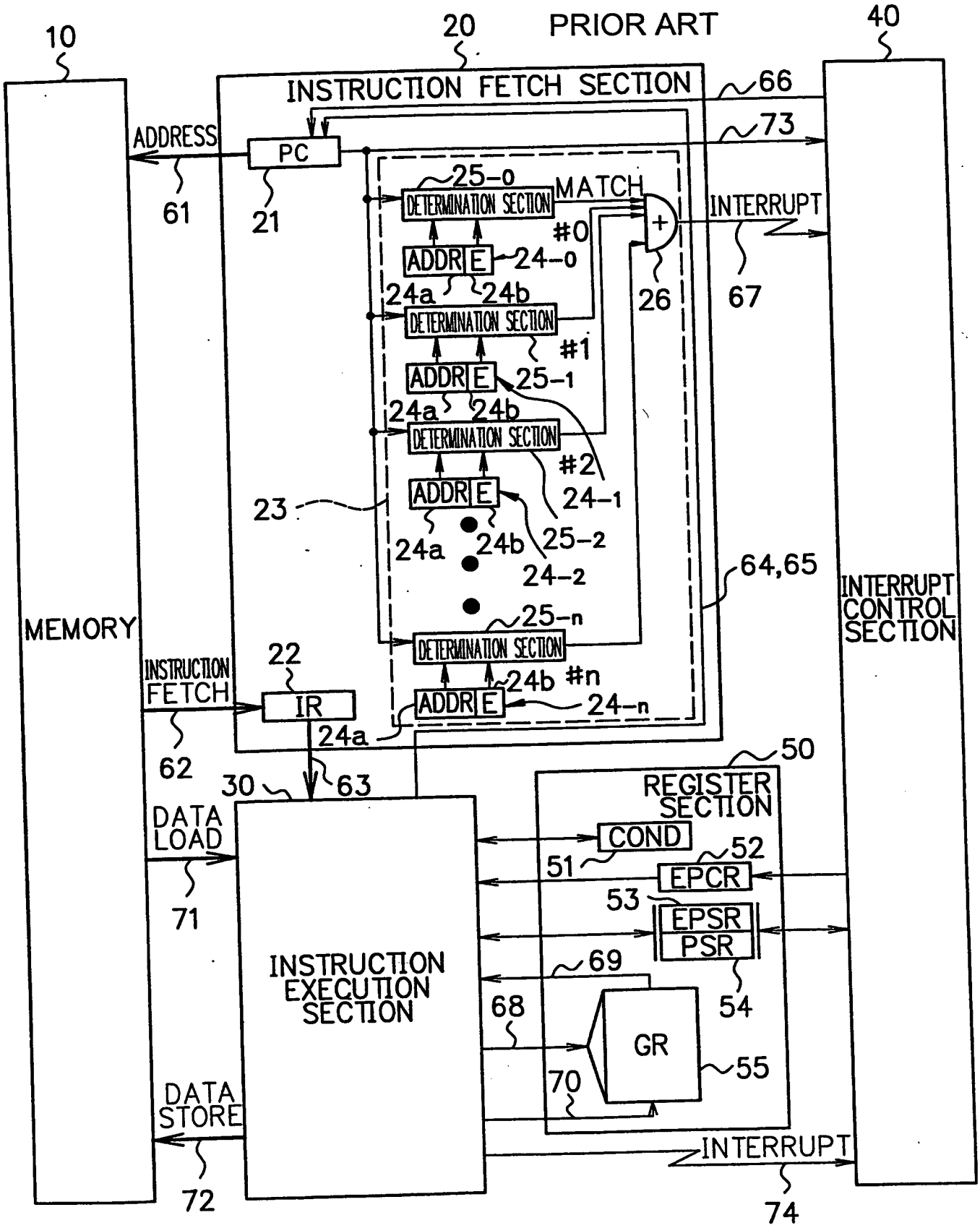


FIG. 2

PRIOR ART



F I G. 3


PRIOR ART
10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
25-0
DETERMINATION SECTION
MATCH
#0
ADDR
E
24-0
24a
24b
INTERRUPT
67
26
DETERMINATION SECTION
#1
ADDR
E
25-1
24a
24b
DETERMINATION SECTION
#2
24-1
23
ADDR
E
24a
24b
25-2
24-2
64,65
INTERRUPT CONTROL SECTION
MEMORY
25-n
DETERMINATION SECTION
22
INSTRUCTION FETCH
IR
24b
#n
ADDR
E
24-n
24a
62
30
63
50
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
68
54
GR
55
70
DATA STORE
INTERRUPT
72
74

F I G. 4

PRIOR ART

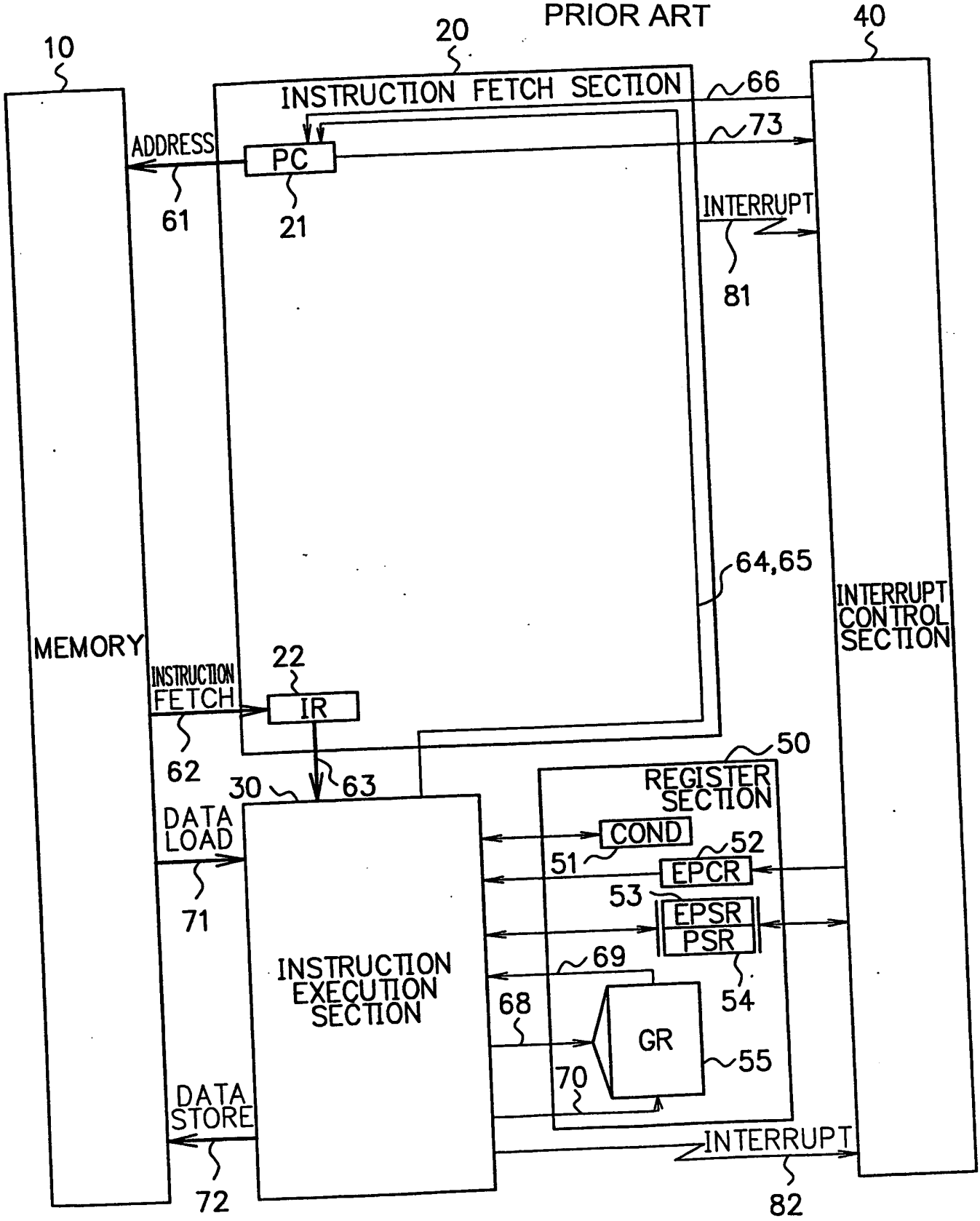


FIG. 5

PRIOR ART

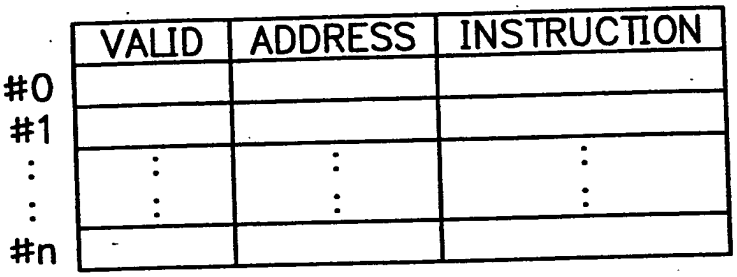


FIG. 6

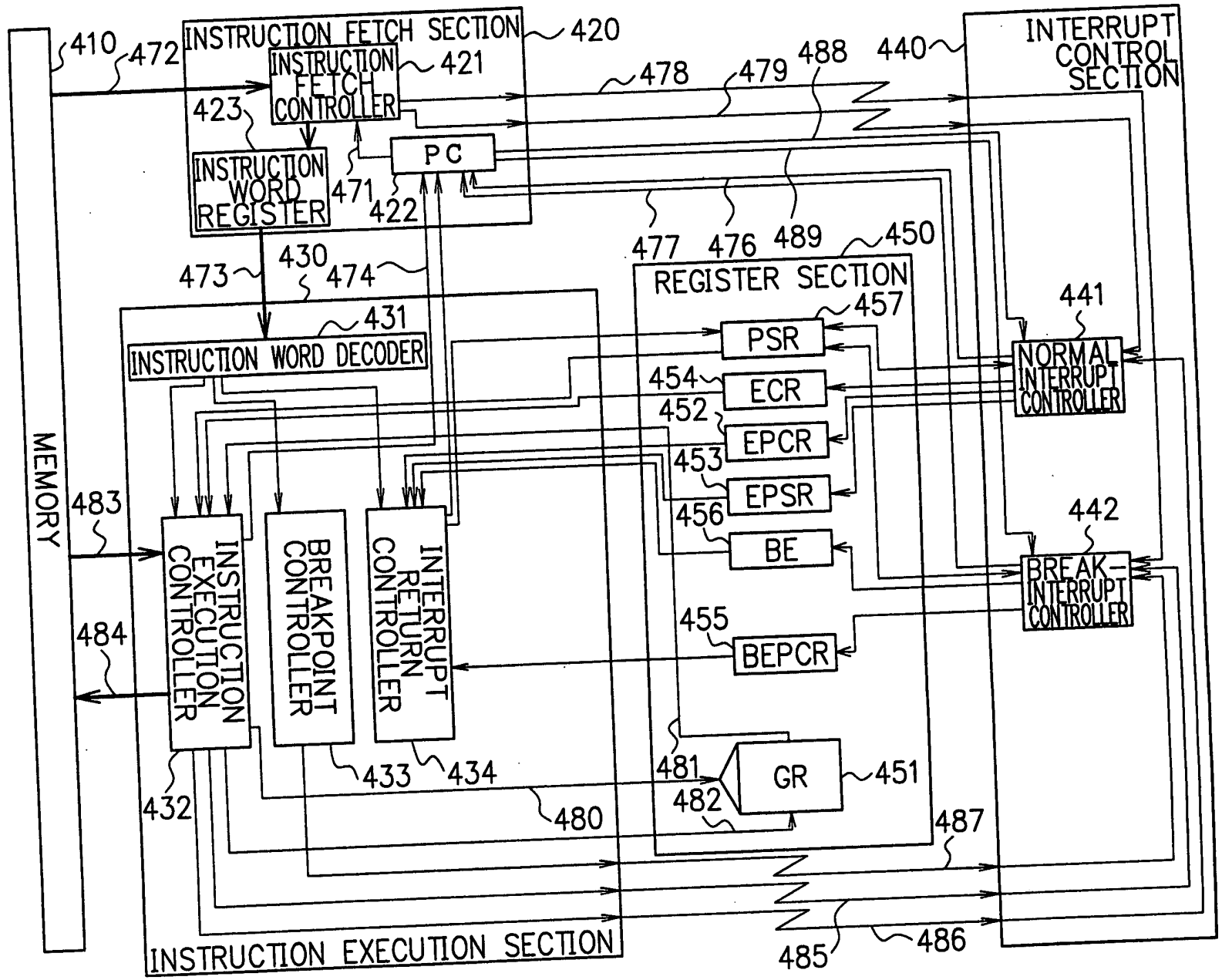

INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
INSTRUCTION WORD REGISTER
PC
INTERRUPT CONTROL SECTION
440
REGISTER SECTION
450
INSTRUCTION WORD DECODER
431
PSR
457
ECR
454
EPCR
452
EPSR
453
BE
456
BEPCR
455
GR
451
NORMAL INTERRUPT CONTROLLER
441
BREAK-INTERRUPT CONTROLLER
442
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
MEMORY
INSTRUCTION EXECUTION SECTION
410
472
423
471
422
478
479
488
477
476
489
473
430
474
483
484
432
433
434
480
481
482
487
485
486

FIG. 7

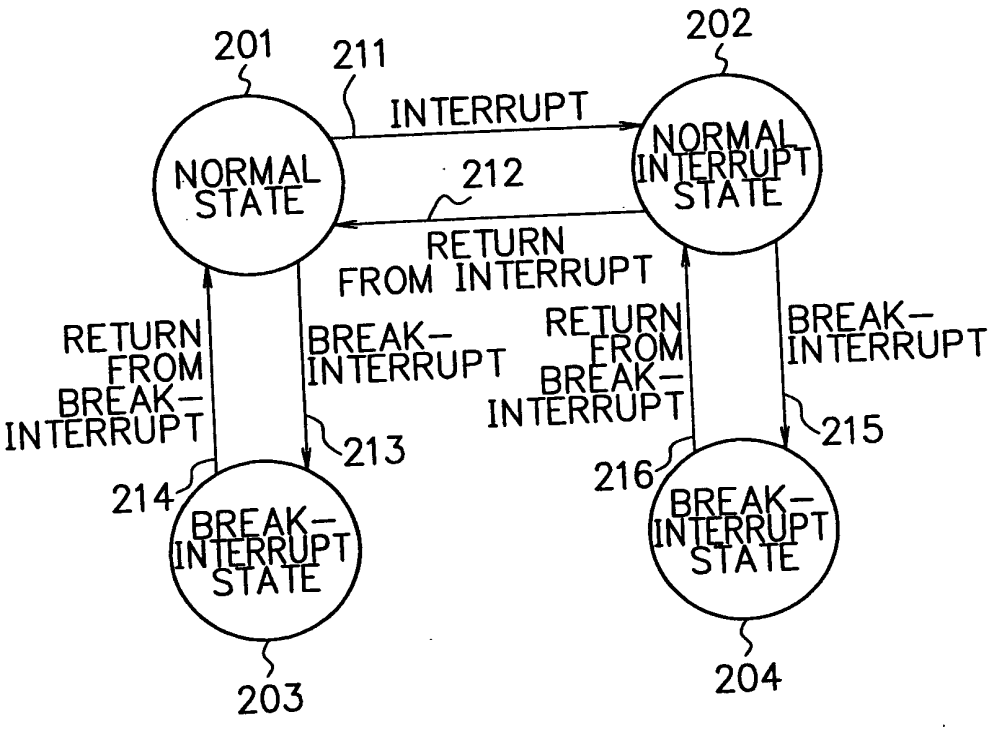

201
211
202
INTERRUPT
NORMAL STATE
212
NORMAL INTERRUPT STATE
RETURN FROM INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
213
215
214
216
BREAK-INTERRUPT STATE
BREAK-INTERRUPT STATE
203
204

FIG. 8

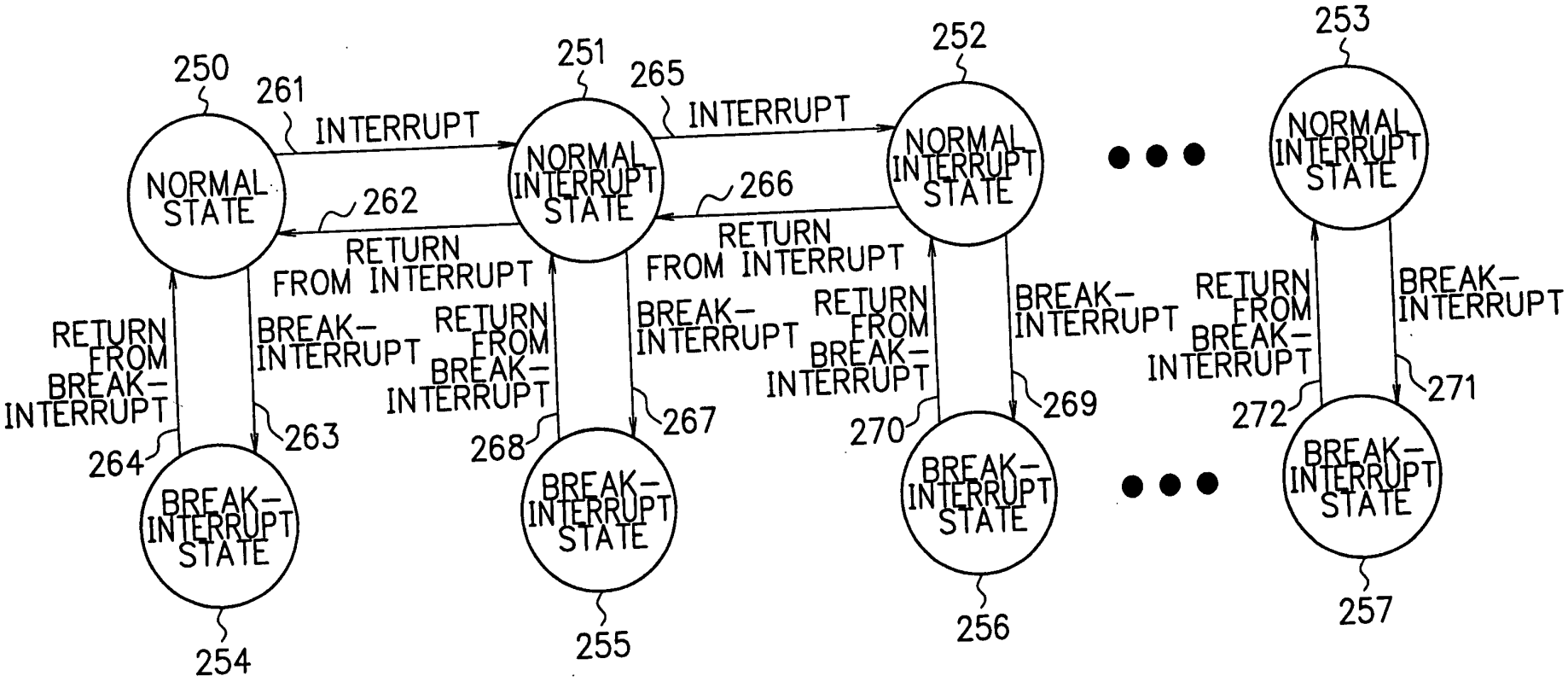

250
251
252
253
261
265
INTERRUPT
INTERRUPT
NORMAL STATE
NORMAL INTERRUPT STATE
NORMAL INTERRUPT STATE
NORMAL INTERRUPT STATE
262
266
RETURN FROM INTERRUPT
RETURN FROM INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
RETURN FROM BREAK-INTERRUPT
BREAK-INTERRUPT
263
264
267
268
269
270
271
272
BREAK-INTERRUPT STATE
BREAK-INTERRUPT STATE
BREAK-INTERRUPT STATE
BREAK-INTERRUPT STATE
254
255
256
257

FIG. 9

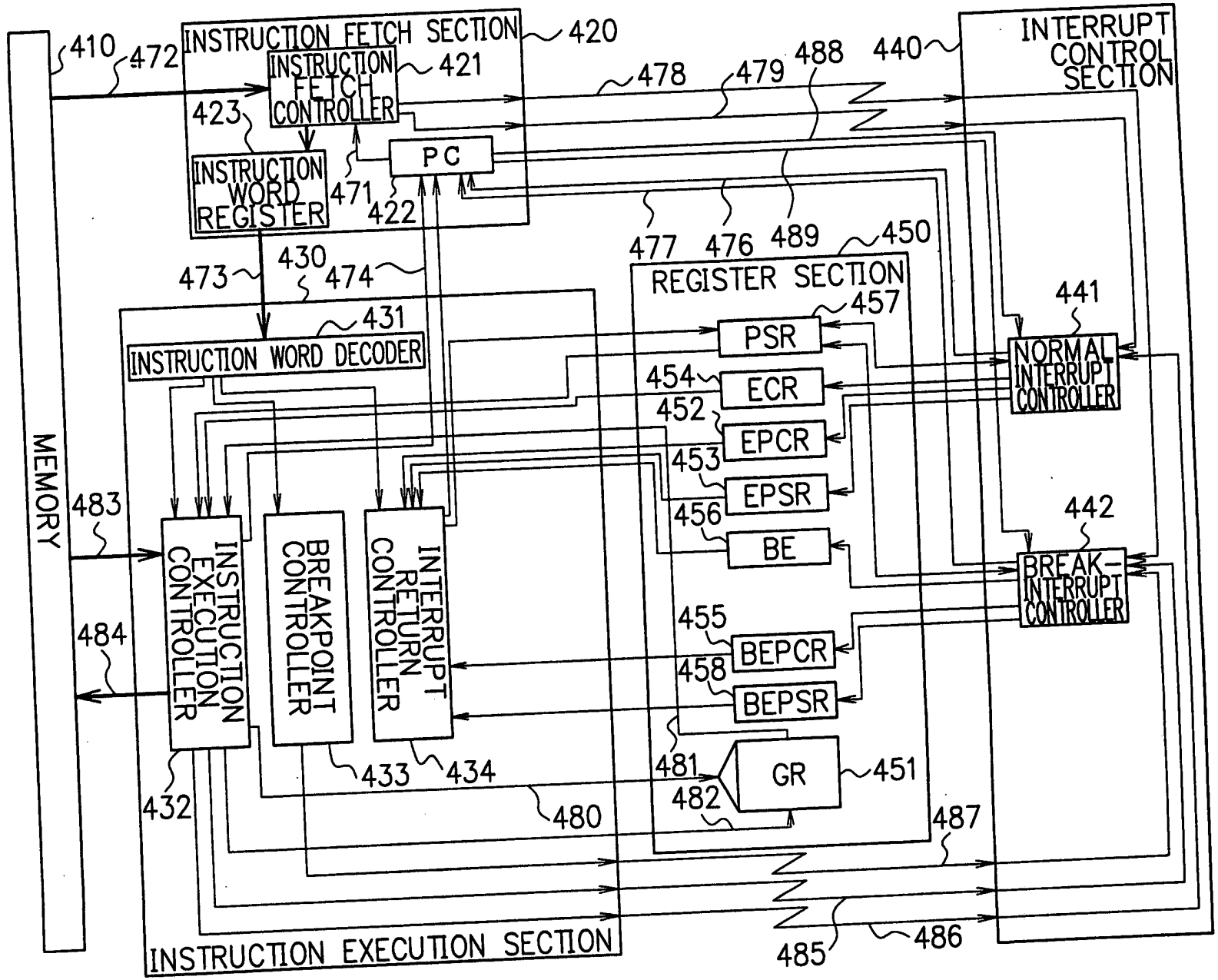
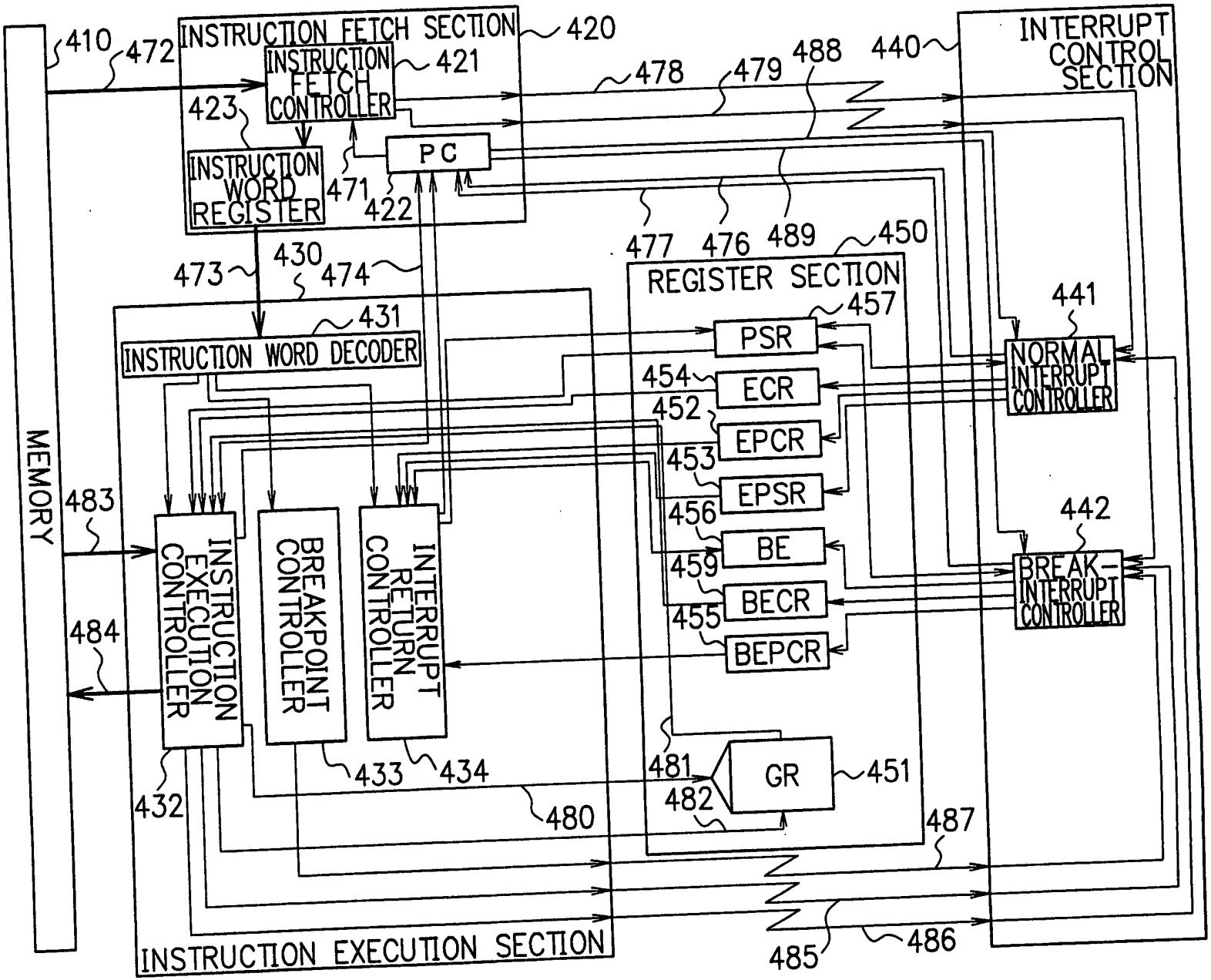

MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
473
430
474
477
476
489
450
REGISTER SECTION
431
INSTRUCTION WORD DECODER
457
PSR
441
NORMAL INTERRUPT CONTROLLER
454
ECR
452
EPCR
453
EPSR
456
BE
442
BREAK-INTERRUPT CONTROLLER
483
484
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
455
BEPCR
458
BEPSR
481
GR
451
482
433
434
432
480
487
485
486
INSTRUCTION EXECUTION SECTION

FIG. 10


MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
473
430
474
477
476
489
450
REGISTER SECTION
431
INSTRUCTION WORD DECODER
457
PSR
441
NORMAL INTERRUPT CONTROLLER
454
ECR
452
EPCR
453
EPSR
456
BE
442
459
BECR
BREAK-INTERRUPT CONTROLLER
455
BEPCR
483
484
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
433
434
432
480
481
482
GR
451
487
INSTRUCTION EXECUTION SECTION
485
486

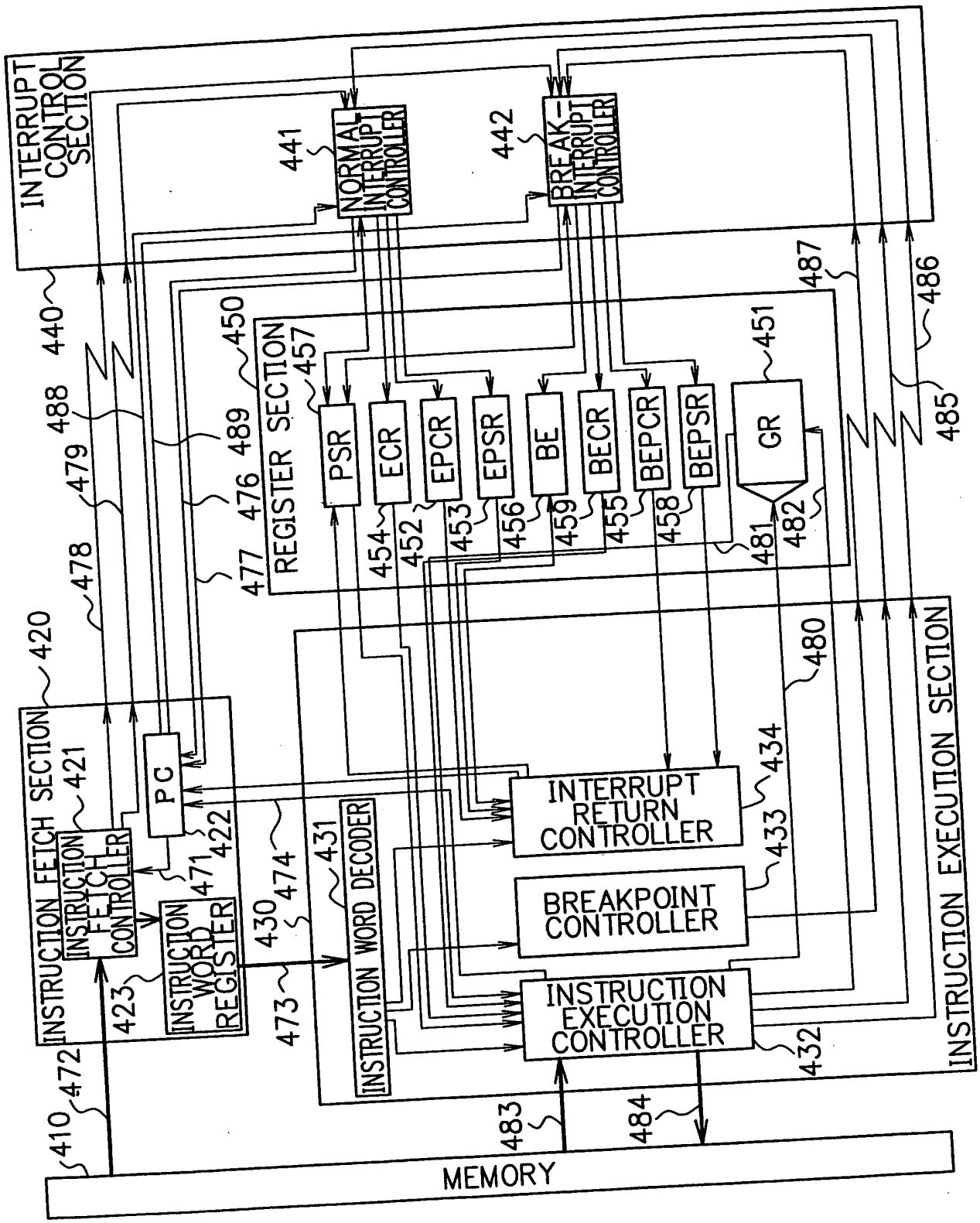

INTERRUPT CONTROL SECTION
NORMAL INTERRUPT CONTROLLER
BREAK INTERRUPT CONTROLLER
REGISTER SECTION
PSR
ECR
EPCR
EPSR
BE
BECR
BEPCR
BEPSR
GR
INSTRUCTION FETCH SECTION
INSTRUCTION FETCH CONTROLLER
PC
INSTRUCTION WORD REGISTER
INSTRUCTION WORD DECODER
INTERRUPT RETURN CONTROLLER
BREAKPOINT CONTROLLER
INSTRUCTION EXECUTION CONTROLLER
INSTRUCTION EXECUTION SECTION
MEMORY

FIG. 11

FIG. 12

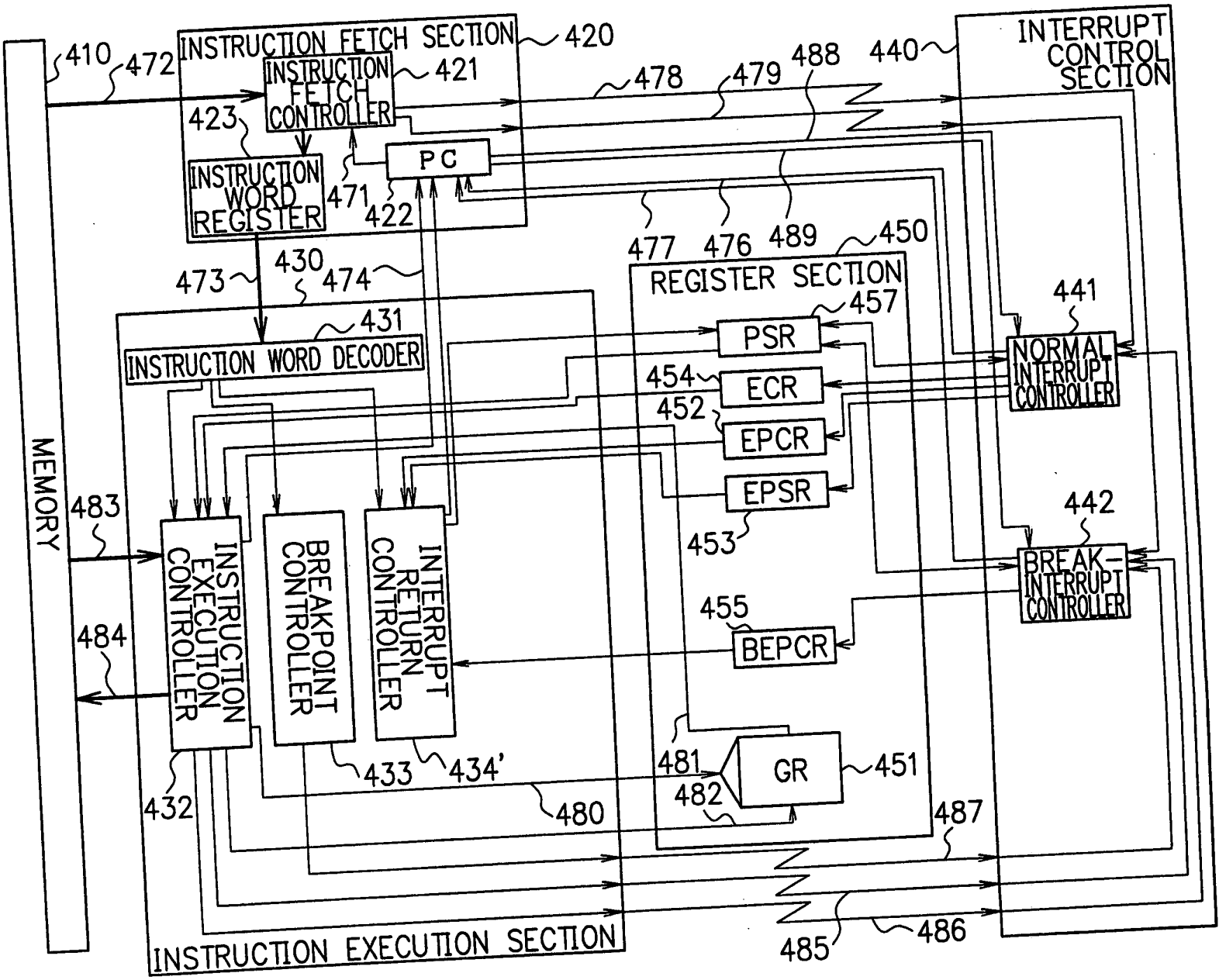

MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
473
430
474
431
INSTRUCTION WORD DECODER
477
476
489
450
REGISTER SECTION
457
PSR
454
ECR
452
EPCR
EPSR
453
441
NORMAL INTERRUPT CONTROLLER
442
BREAK-INTERRUPT CONTROLLER
455
BEPCR
483
484
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
481
482
GR
451
432
433
434'
480
487
485
486
INSTRUCTION EXECUTION SECTION

FIG. 13

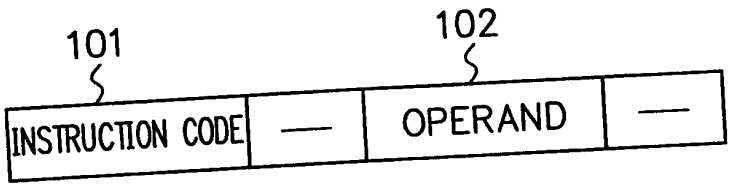


FIG. 14

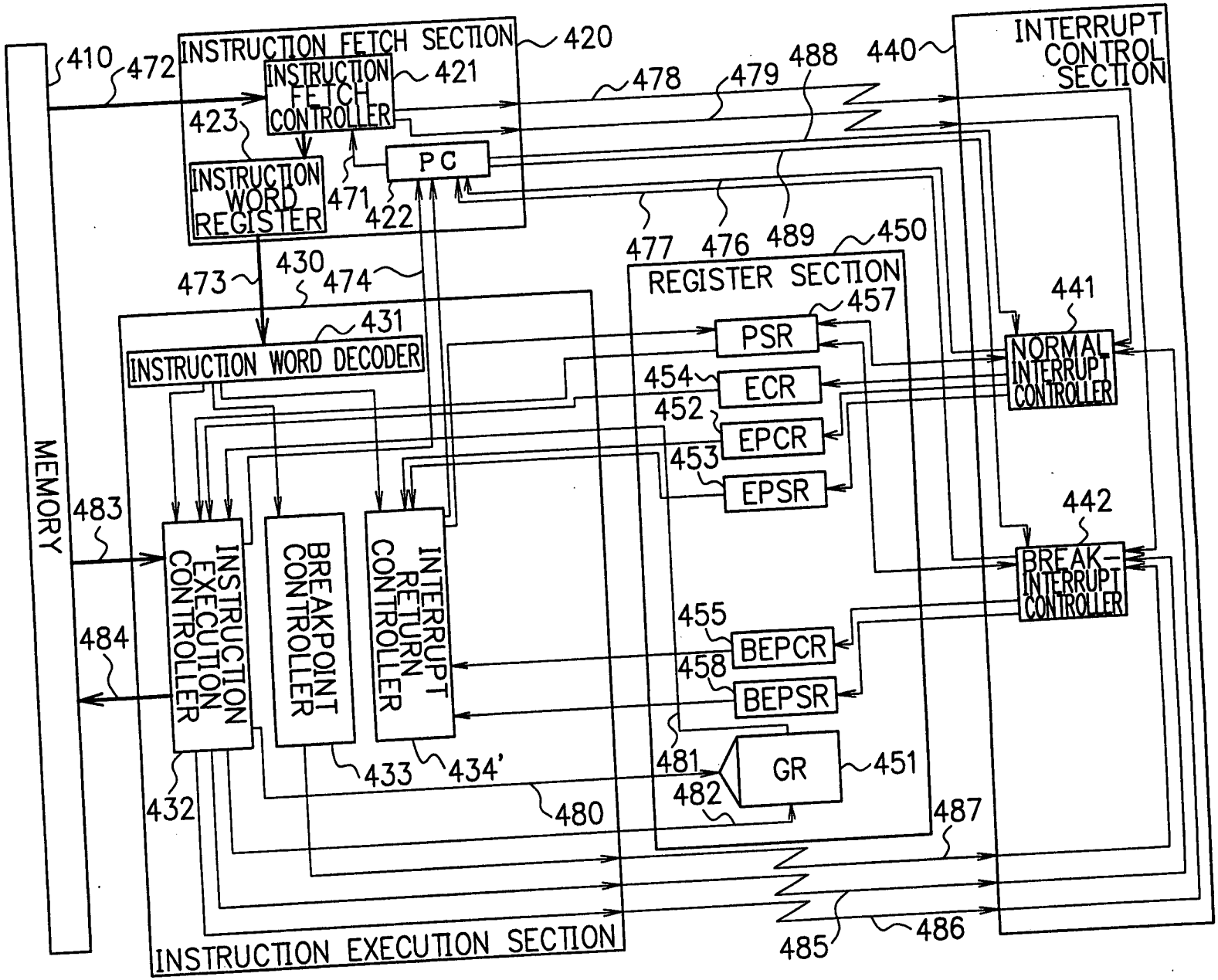

MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
473
430
474
431
INSTRUCTION WORD DECODER
477
476
489
450
REGISTER SECTION
457
PSR
454
ECR
452
EPCR
453
EPSR
441
NORMAL INTERRUPT CONTROLLER
483
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
442
BREAK-INTERRUPT CONTROLLER
455
BEPCR
458
BEPSR
484
481
GR
451
482
432
433
434'
480
487
485
486
INSTRUCTION EXECUTION SECTION

FIG. 15

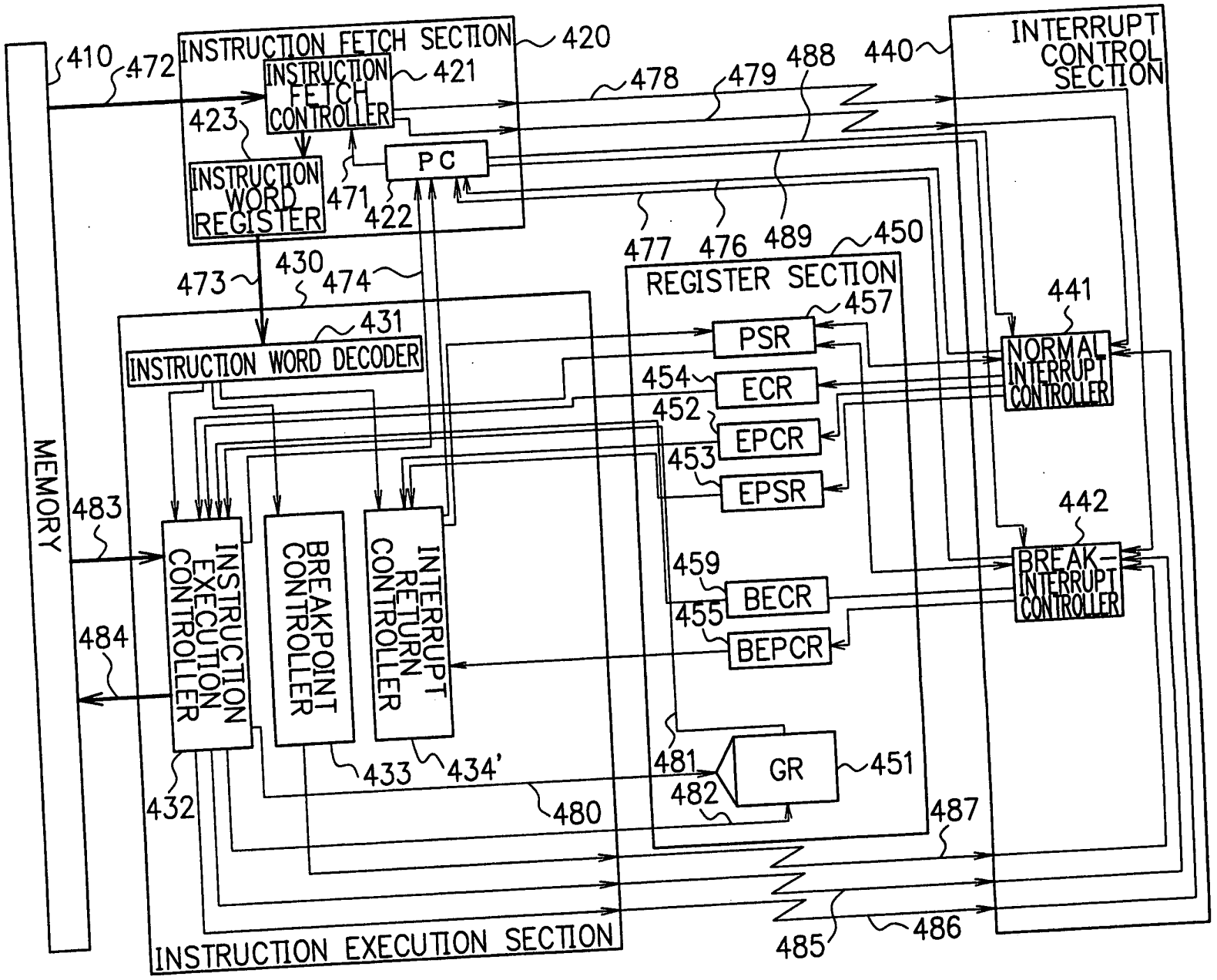

MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
473
430
474
431
INSTRUCTION WORD DECODER
477
476
489
450
REGISTER SECTION
457
PSR
454
ECR
452
EPCR
453
EPSR
441
NORMAL INTERRUPT CONTROLLER
442
BREAK-INTERRUPT CONTROLLER
459
BECR
455
BEPCR
483
484
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
481
482
GR
451
432
433
434'
480
487
485
486
INSTRUCTION EXECUTION SECTION

FIG. 16

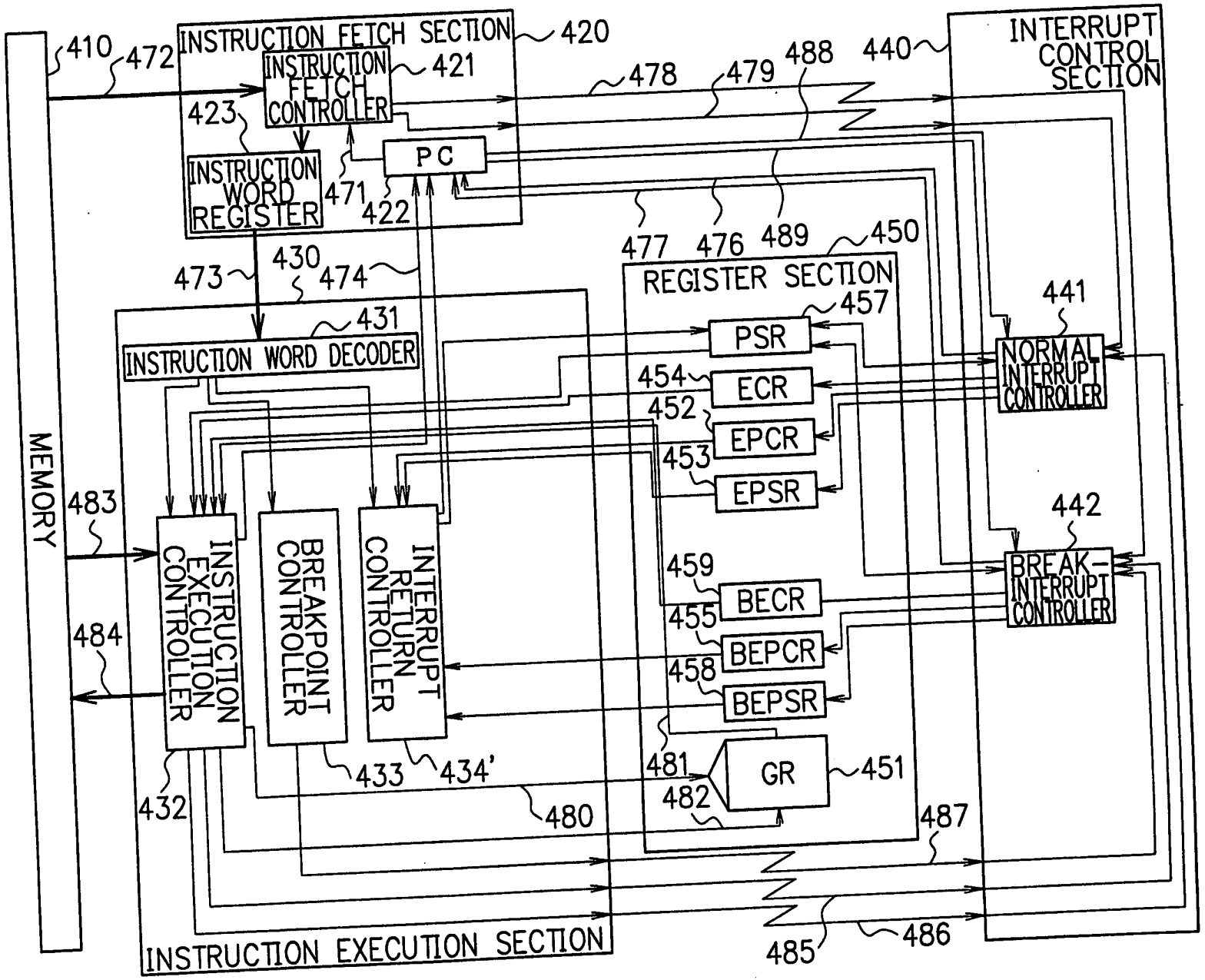
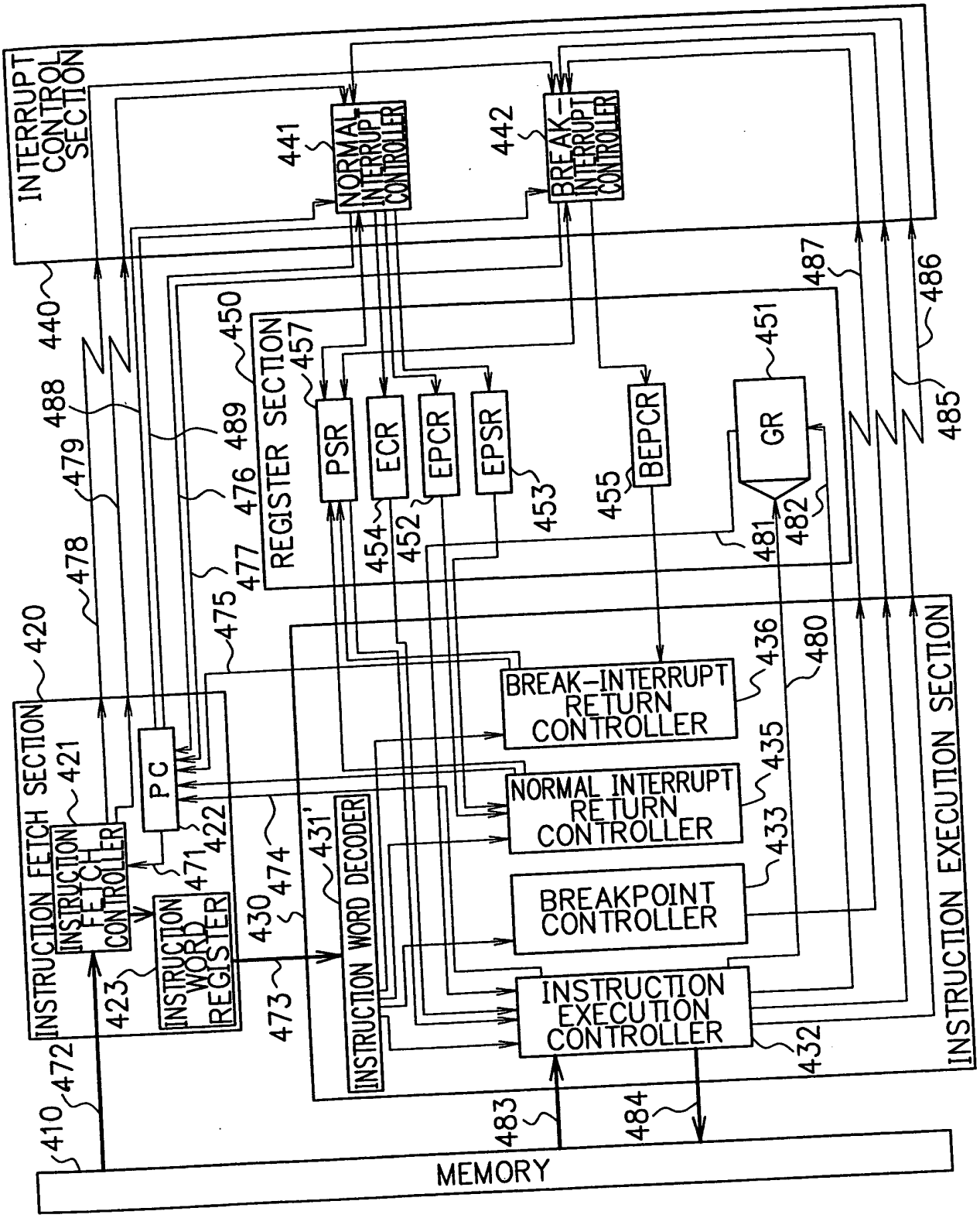

MEMORY
410
472
INSTRUCTION FETCH SECTION
420
INSTRUCTION FETCH CONTROLLER
421
423
INSTRUCTION WORD REGISTER
471
PC
422
478
479
488
440
INTERRUPT CONTROL SECTION
477
476
489
450
REGISTER SECTION
473
430
474
431
INSTRUCTION WORD DECODER
457
PSR
441
NORMAL INTERRUPT CONTROLLER
454
ECR
452
EPCR
453
EPSR
483
INSTRUCTION EXECUTION CONTROLLER
BREAKPOINT CONTROLLER
INTERRUPT RETURN CONTROLLER
442
BREAK-INTERRUPT CONTROLLER
459
BECR
455
BEPCR
458
BEPSR
484
481
GR
451
482
432
433
434'
480
487
485
486
INSTRUCTION EXECUTION SECTION

FIG. 17


INTERRUPT CONTROL SECTION
NORMAL INTERRUPT CONTROLLER
BREAK-INTERRUPT CONTROLLER
REGISTER SECTION
PSR
ECR
EPCR
EPSR
BEPCR
GR
INSTRUCTION FETCH SECTION
INSTRUCTION FETCH CONTROLLER
PC
INSTRUCTION WORD REGISTER
INSTRUCTION WORD DECODER
BREAK-INTERRUPT RETURN CONTROLLER
NORMAL INTERRUPT RETURN CONTROLLER
BREAKPOINT CONTROLLER
INSTRUCTION EXECUTION CONTROLLER
INSTRUCTION EXECUTION SECTION
MEMORY
410
420
421
422
423
430
431'
432
433
435
436
440
441
442
450
451
452
453
454
455
457
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489

F I G. 18

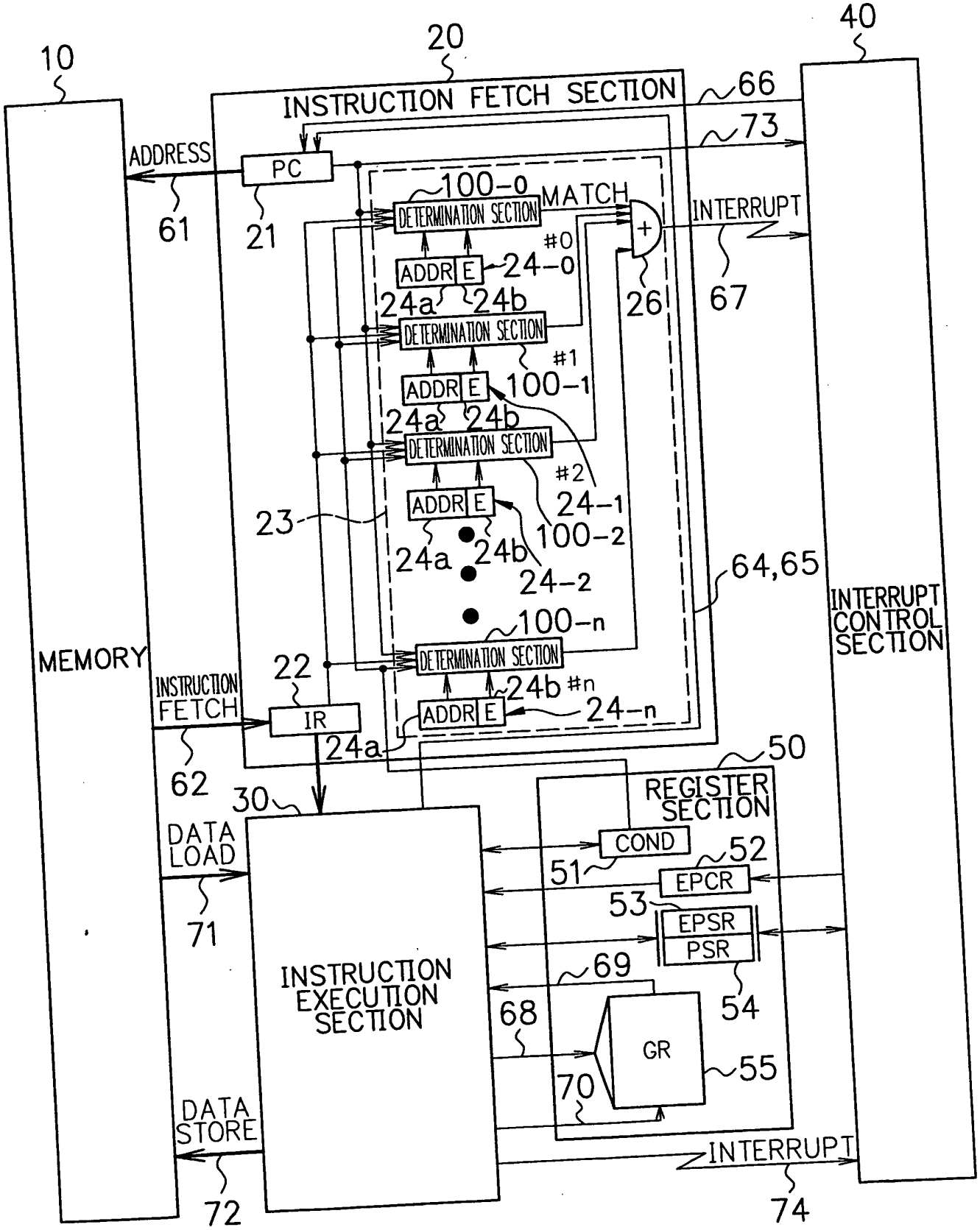
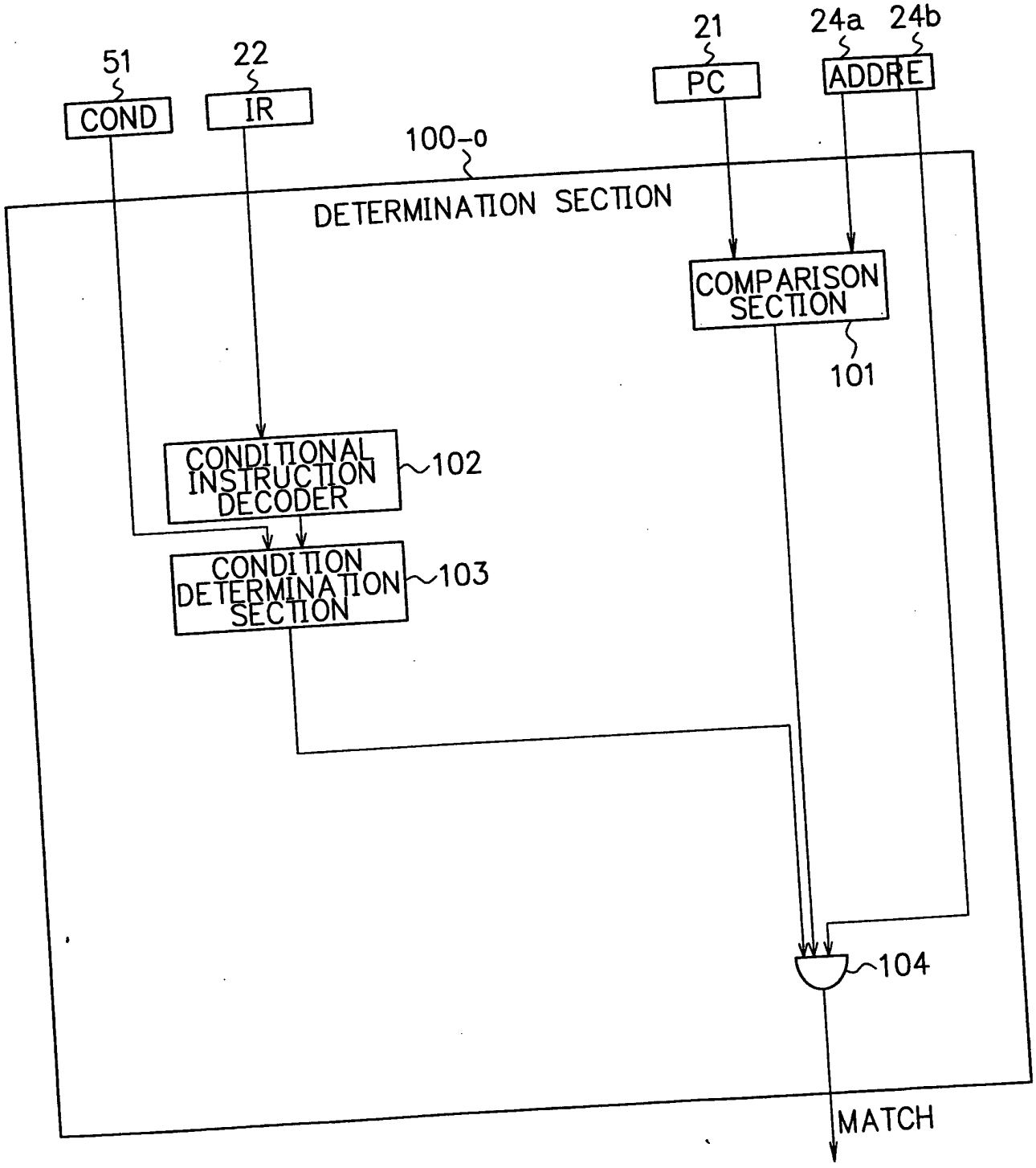

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
100-0
MATCH
DETERMINATION SECTION
INTERRUPT
#0
ADDR
E
24-0
24a
24b
26
67
DETERMINATION SECTION
#1
ADDR
E
100-1
24a
24b
DETERMINATION SECTION
#2
ADDR
E
24-1
23
100-2
24a
24b
24-2
64,65
INTERRUPT CONTROL SECTION
100-n
MEMORY
DETERMINATION SECTION
22
INSTRUCTION FETCH
24b
#n
ADDR
E
24-n
IR
24a
62
50
30
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
68
54
GR
55
70
DATA STORE
INTERRUPT
72
74

FIG. 19


51
COND
22
IR
21
PC
24a
24b
ADDRE
100-o
DETERMINATION SECTION
COMPARISON SECTION
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
104
MATCH

F I G. 20

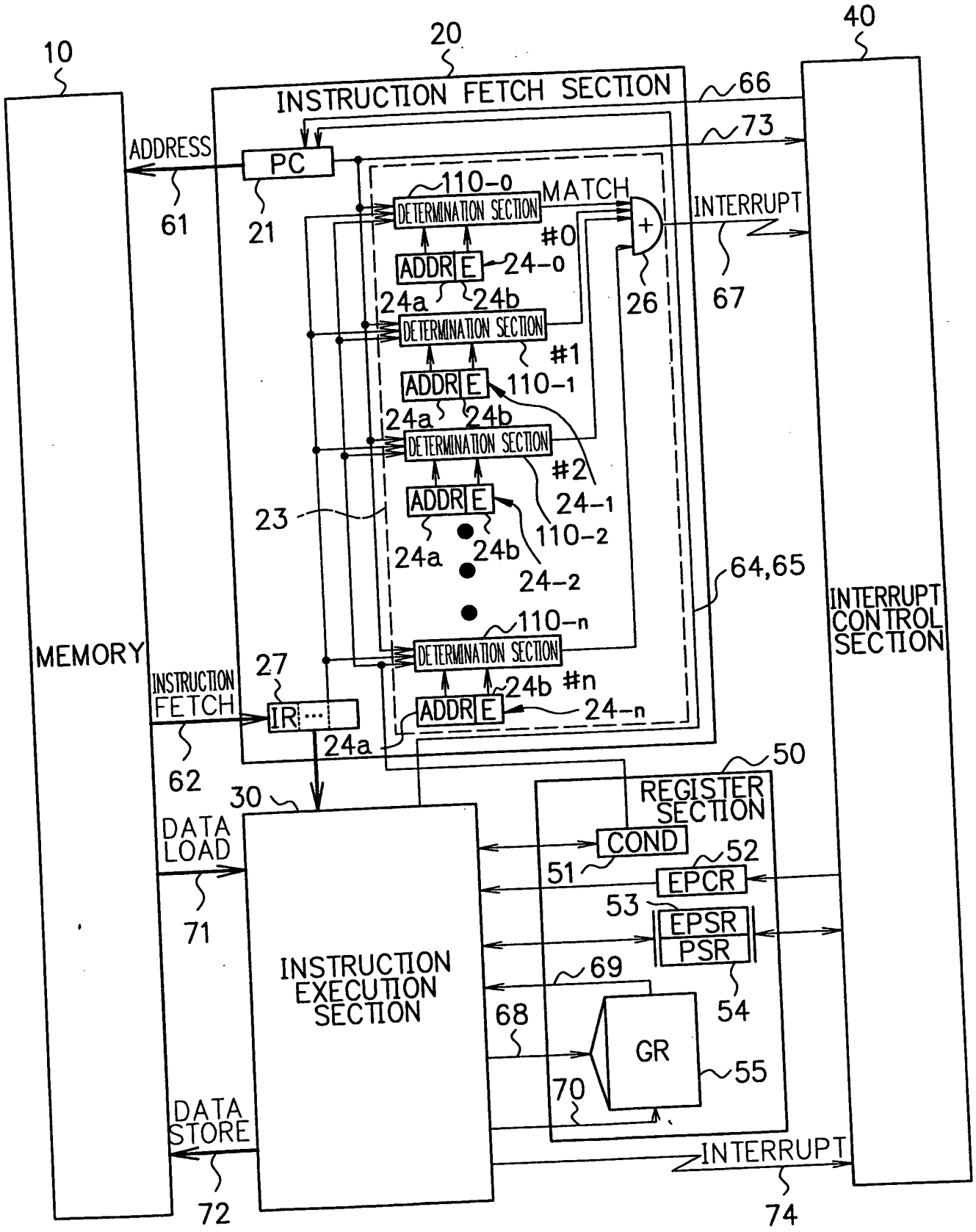
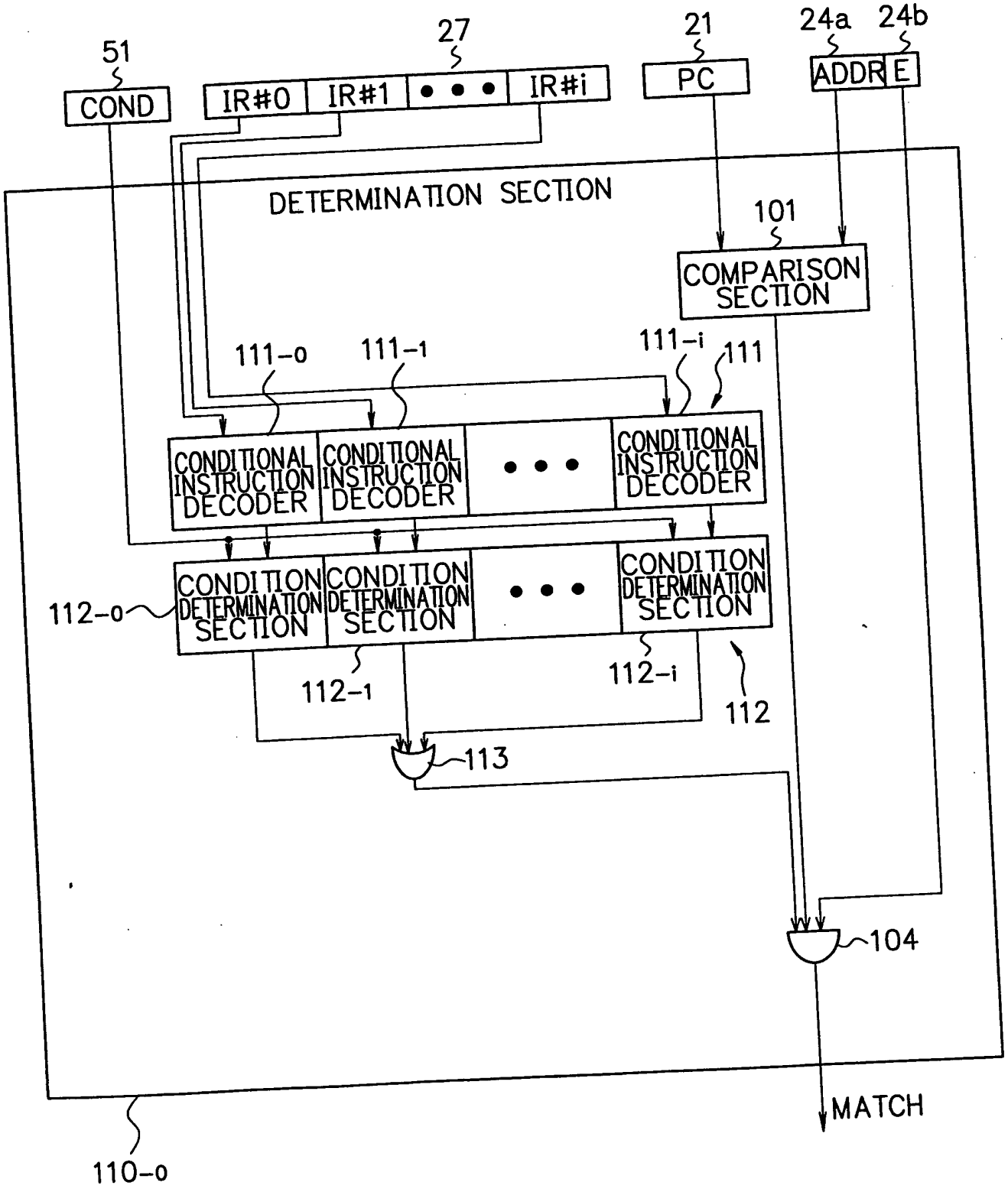

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
110-0
MATCH
DETERMINATION SECTION
#0
INTERRUPT
67
26
ADDR
E
24-0
24a
24b
DETERMINATION SECTION
#1
110-1
DETERMINATION SECTION
#2
24-1
110-2
23
24-2
64,65
110-n
DETERMINATION SECTION
#n
24b
24-n
MEMORY
27
INSTRUCTION FETCH
IR
62
30
50
REGISTER SECTION
DATA LOAD
71
COND
51
52
EPCR
53
EPSR
PSR
54
69
INSTRUCTION EXECUTION SECTION
68
GR
55
70
DATA STORE
72
INTERRUPT
74
INTERRUPT CONTROL SECTION

FIG. 21


51
COND
27
IR#0
IR#1
IR#i
21
PC
24a
24b
ADDR
E
DETERMINATION SECTION
101
COMPARISON SECTION
111-o
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
112-o
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
112-1
112-i
112
113
104
MATCH
110-o

F I G. 22

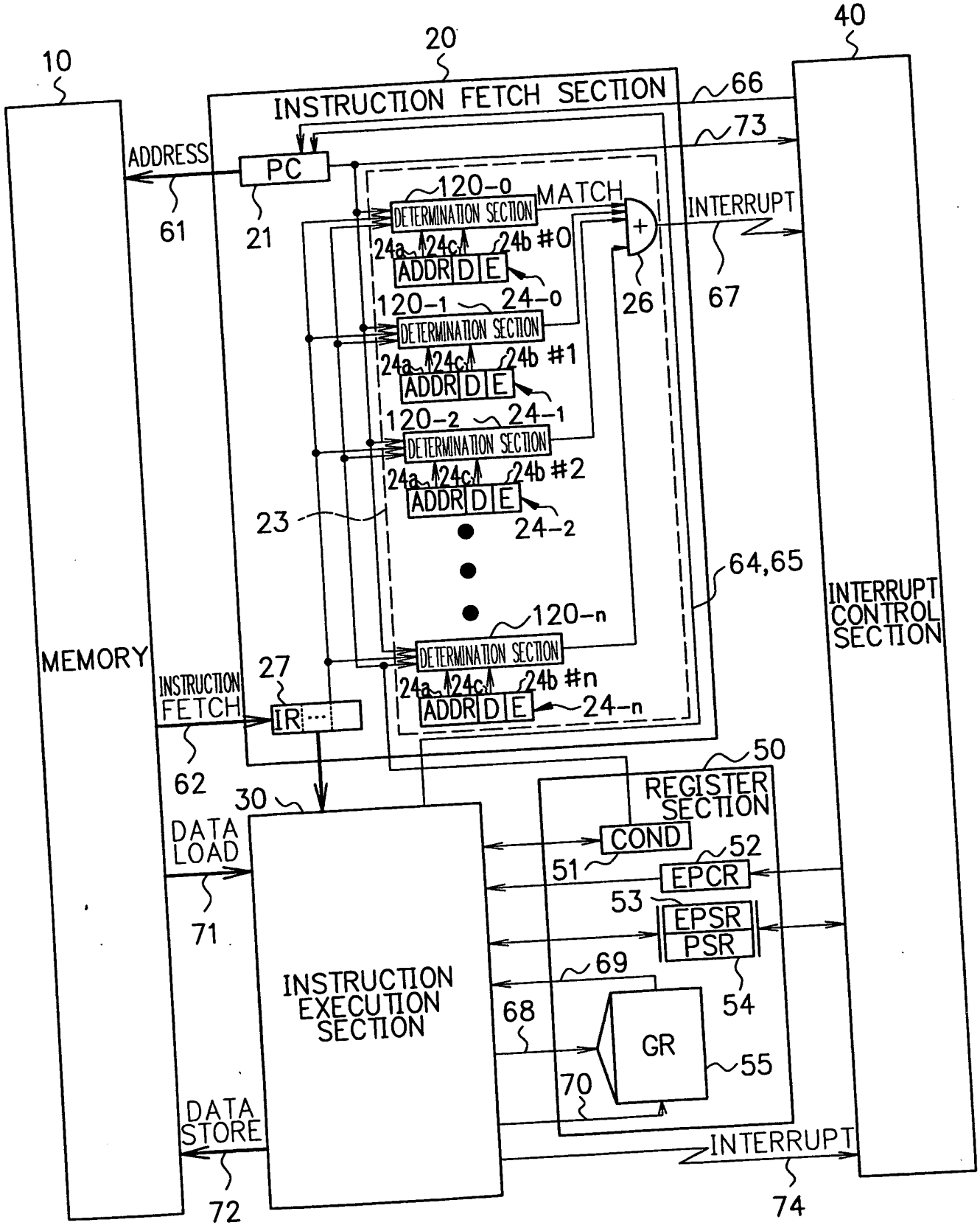
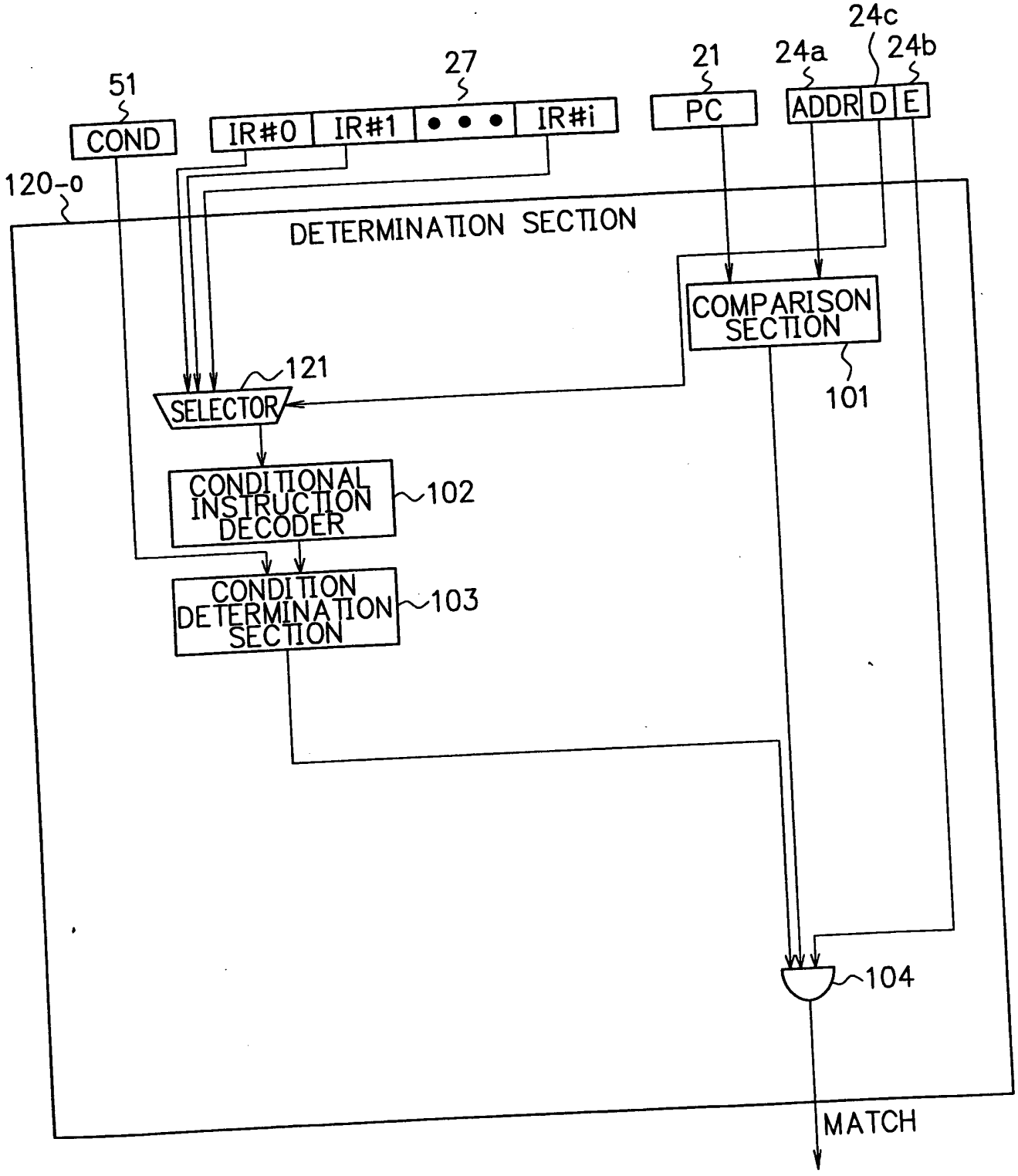

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
120-0
MATCH
DETERMINATION SECTION
24a
24c
24b #0
ADDR D E
24-0
INTERRUPT
67
26
120-1
DETERMINATION SECTION
24b #1
24-1
120-2
DETERMINATION SECTION
24b #2
24-2
23
64,65
120-n
DETERMINATION SECTION
24b #n
24-n
INTERRUPT CONTROL SECTION
MEMORY
27
INSTRUCTION FETCH
IR
62
30
50
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
54
69
INSTRUCTION EXECUTION SECTION
68
GR
55
70
DATA STORE
71
72
INTERRUPT
74

FIG. 23


24c
24a
24b
21
27
51
ADDR
D
E
PC
IR#0
IR#1
IR#i
COND
120-o
DETERMINATION SECTION
COMPARISON SECTION
101
121
SELECTOR
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
104
MATCH

F I G. 24

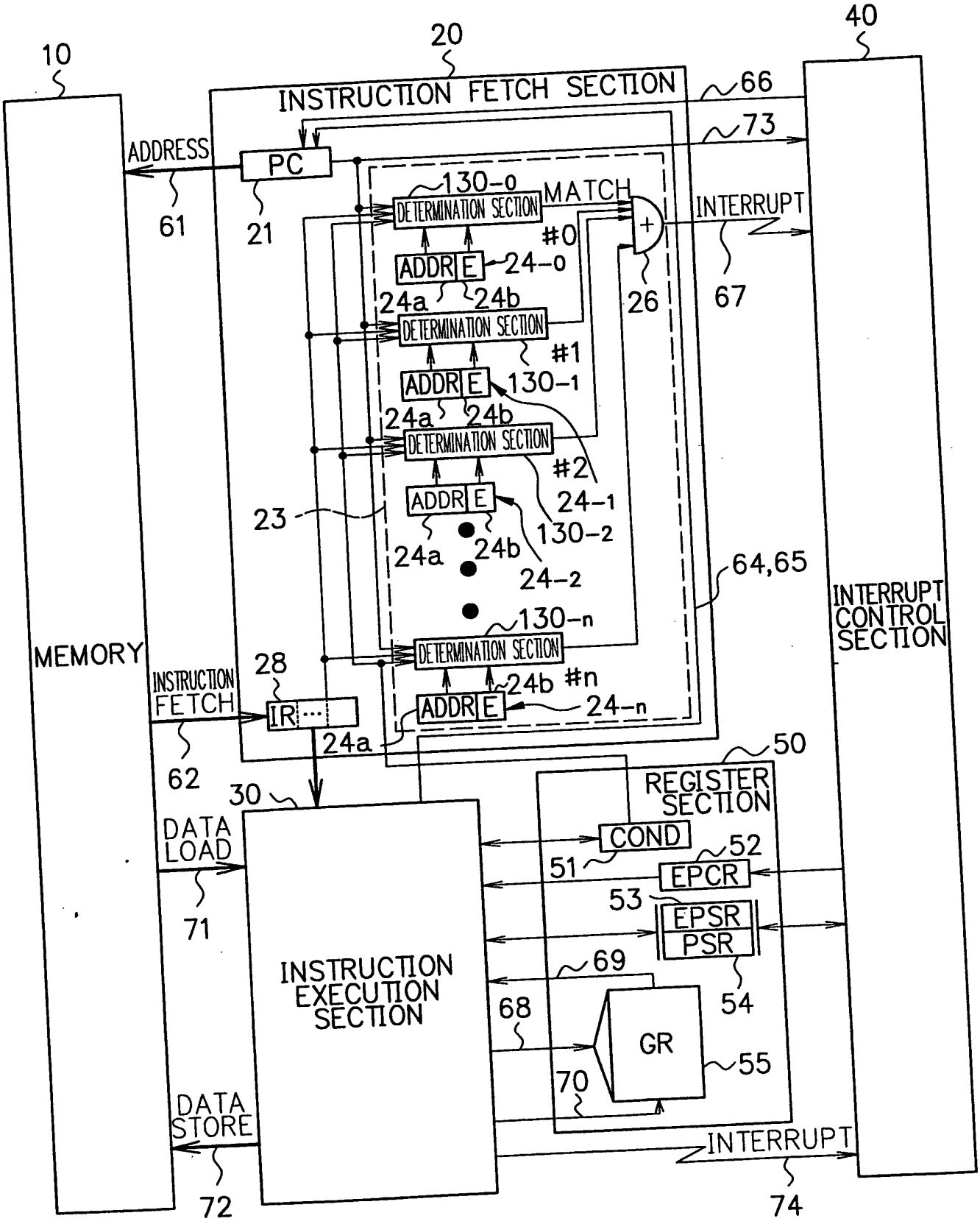

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
130-0
MATCH
DETERMINATION SECTION
#0
INTERRUPT
ADDR
E
24-0
24a
24b
26
67
DETERMINATION SECTION
#1
ADDR
E
130-1
24a
24b
DETERMINATION SECTION
#2
ADDR
E
24-1
23
130-2
24a
24b
24-2
64,65
INTERRUPT CONTROL SECTION
130-n
MEMORY
DETERMINATION SECTION
28
INSTRUCTION FETCH
24b
#n
ADDR
E
24-n
IR
24a
62
50
30
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
54
68
GR
55
70
DATA STORE
INTERRUPT
72
74

FIG. 25

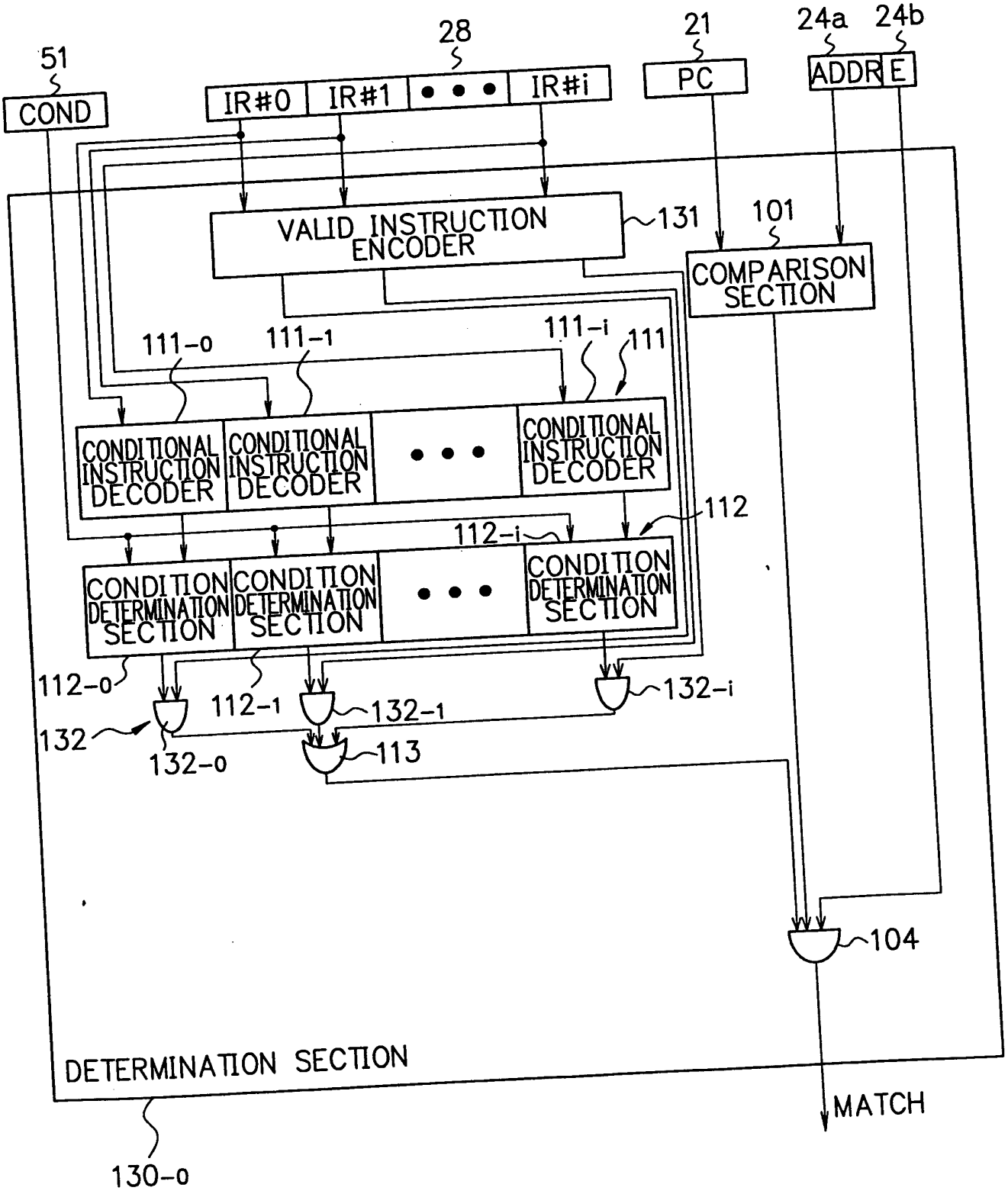
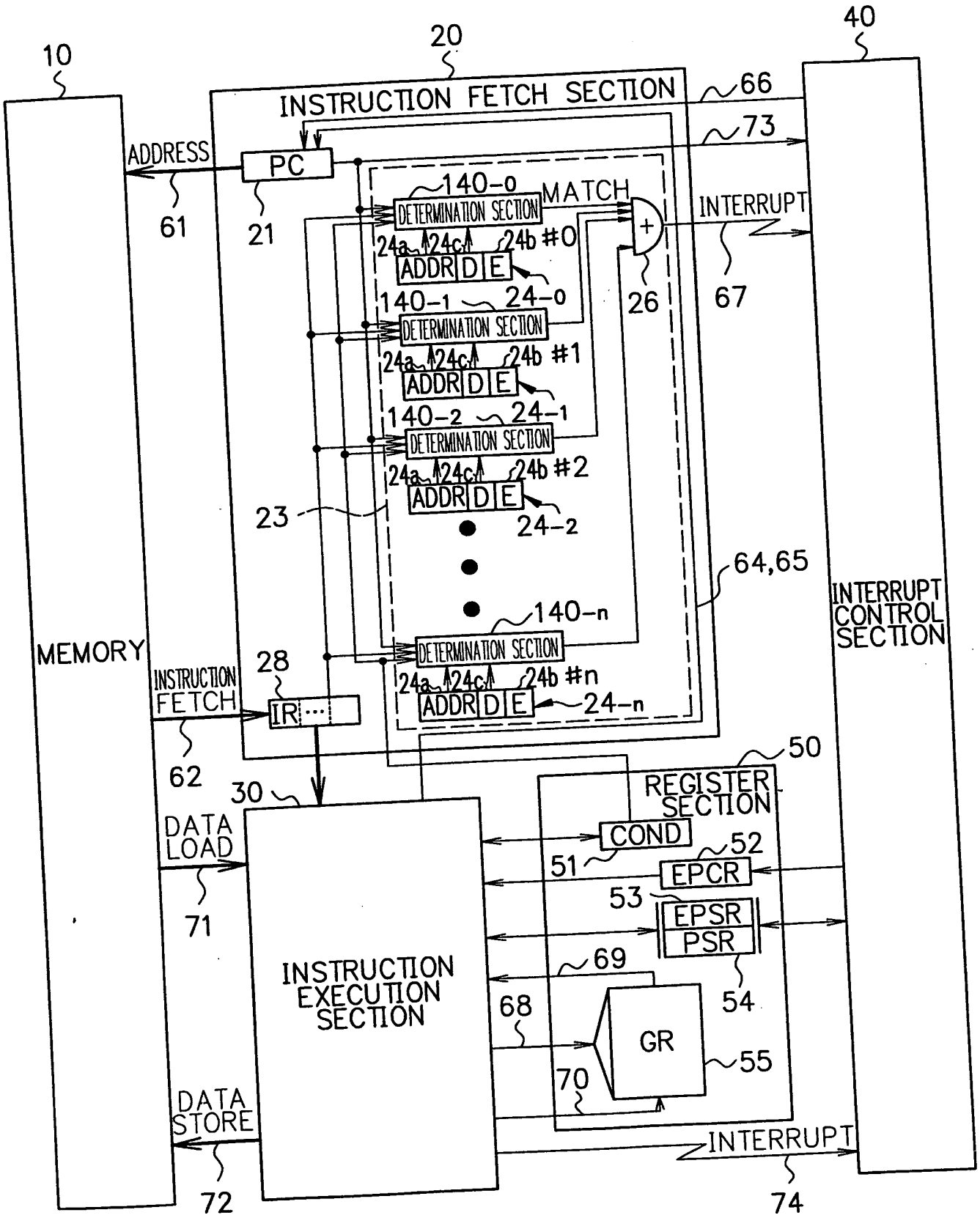
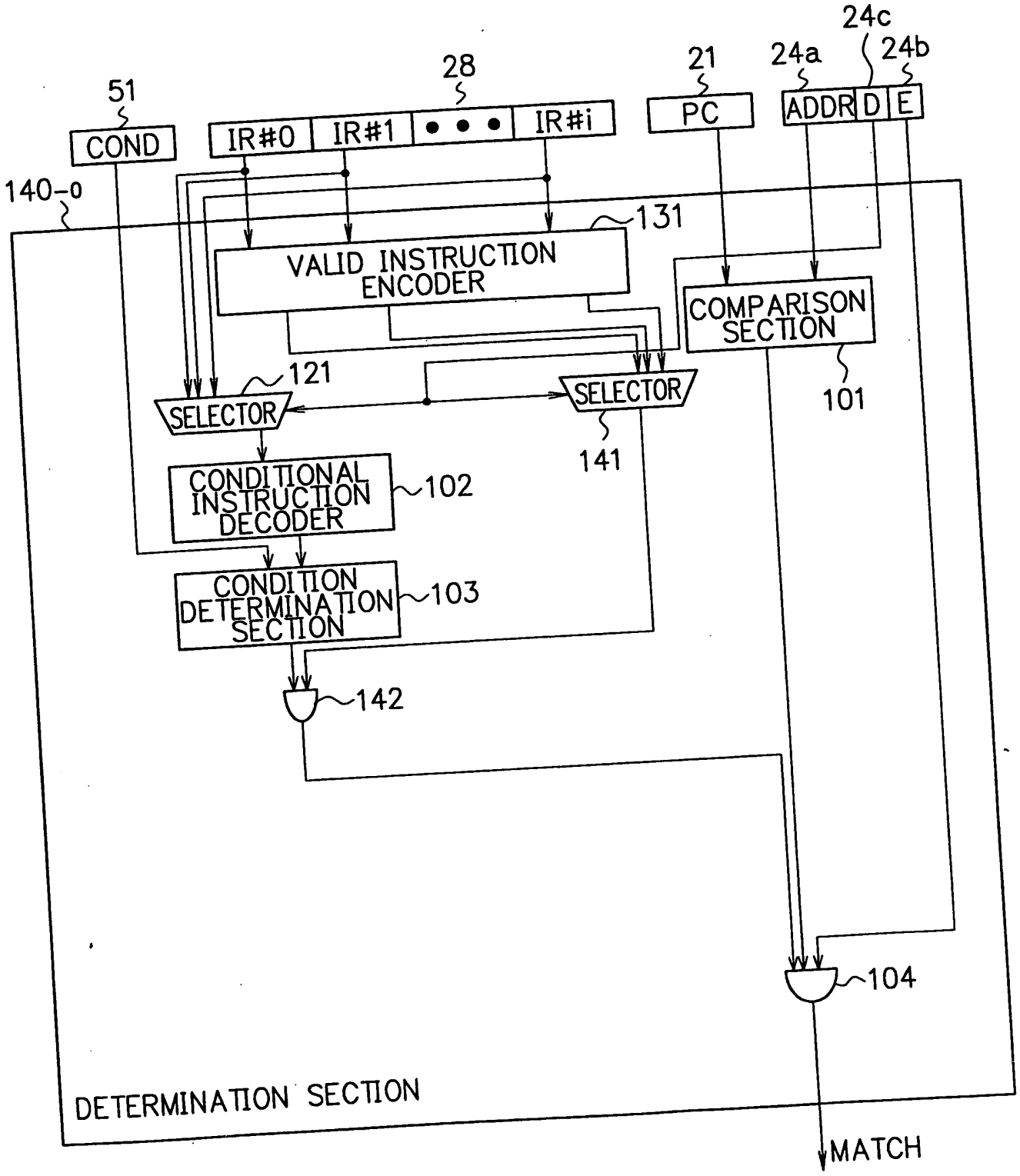

51
COND
28
IR#0
IR#1
IR#i
21
PC
24a
24b
ADDR
E
VALID INSTRUCTION ENCODER
131
101
COMPARISON SECTION
111-0
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
112
112-i
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
112-0
112-1
132-1
132-i
132
132-0
113
104
DETERMINATION SECTION
MATCH
130-0

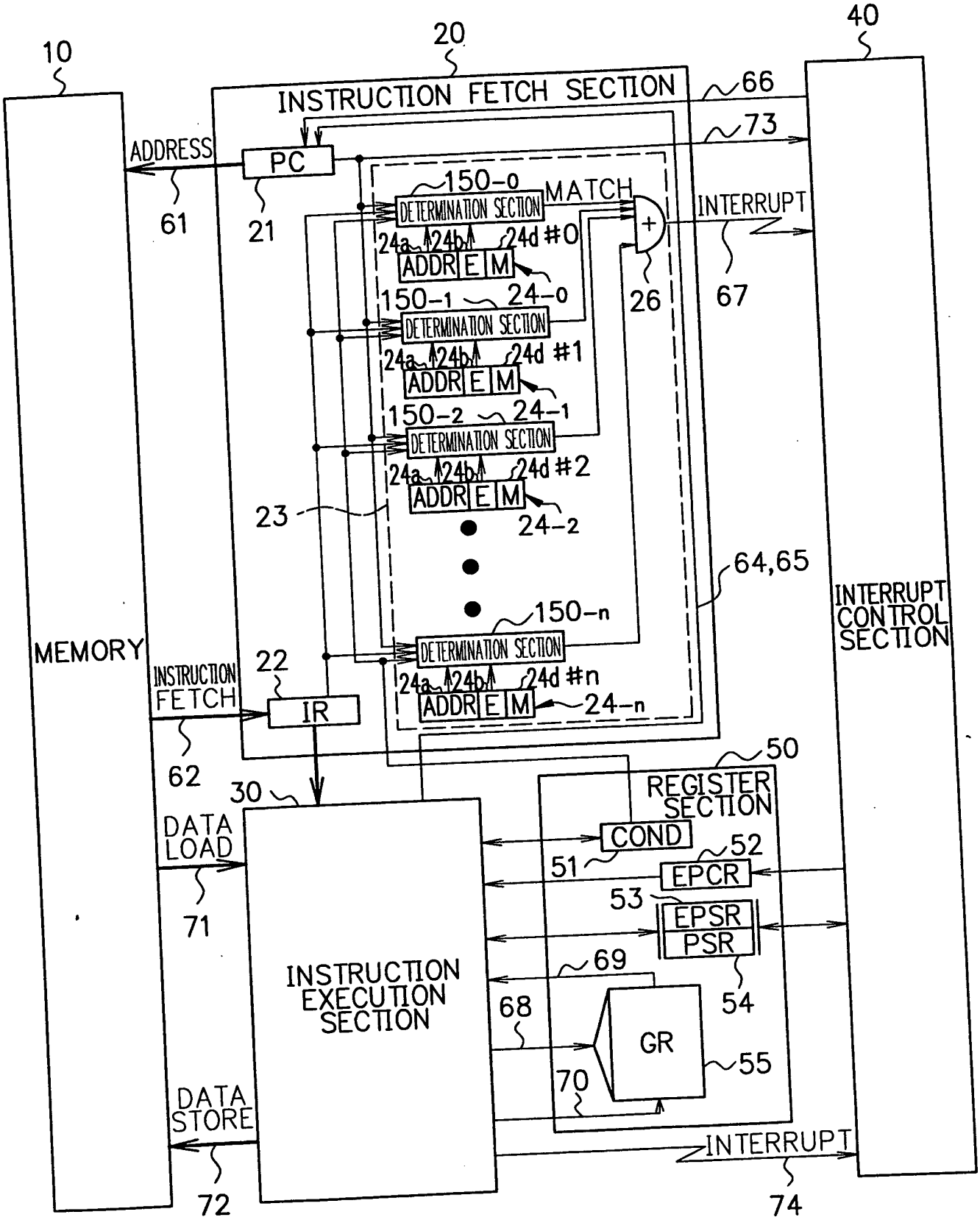
FIG. 26


10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
140-0
MATCH
DETERMINATION SECTION
INTERRUPT
24a
24c
24b #0
ADDR D E
140-1
24-0
26
67
DETERMINATION SECTION
24b #1
140-2
24-1
DETERMINATION SECTION
24b #2
23
24-2
64,65
INTERRUPT CONTROL SECTION
140-n
MEMORY
28
DETERMINATION SECTION
24b #n
INSTRUCTION FETCH
IR
24-n
62
30
50
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
68
54
GR
55
70
DATA STORE
INTERRUPT
72
74

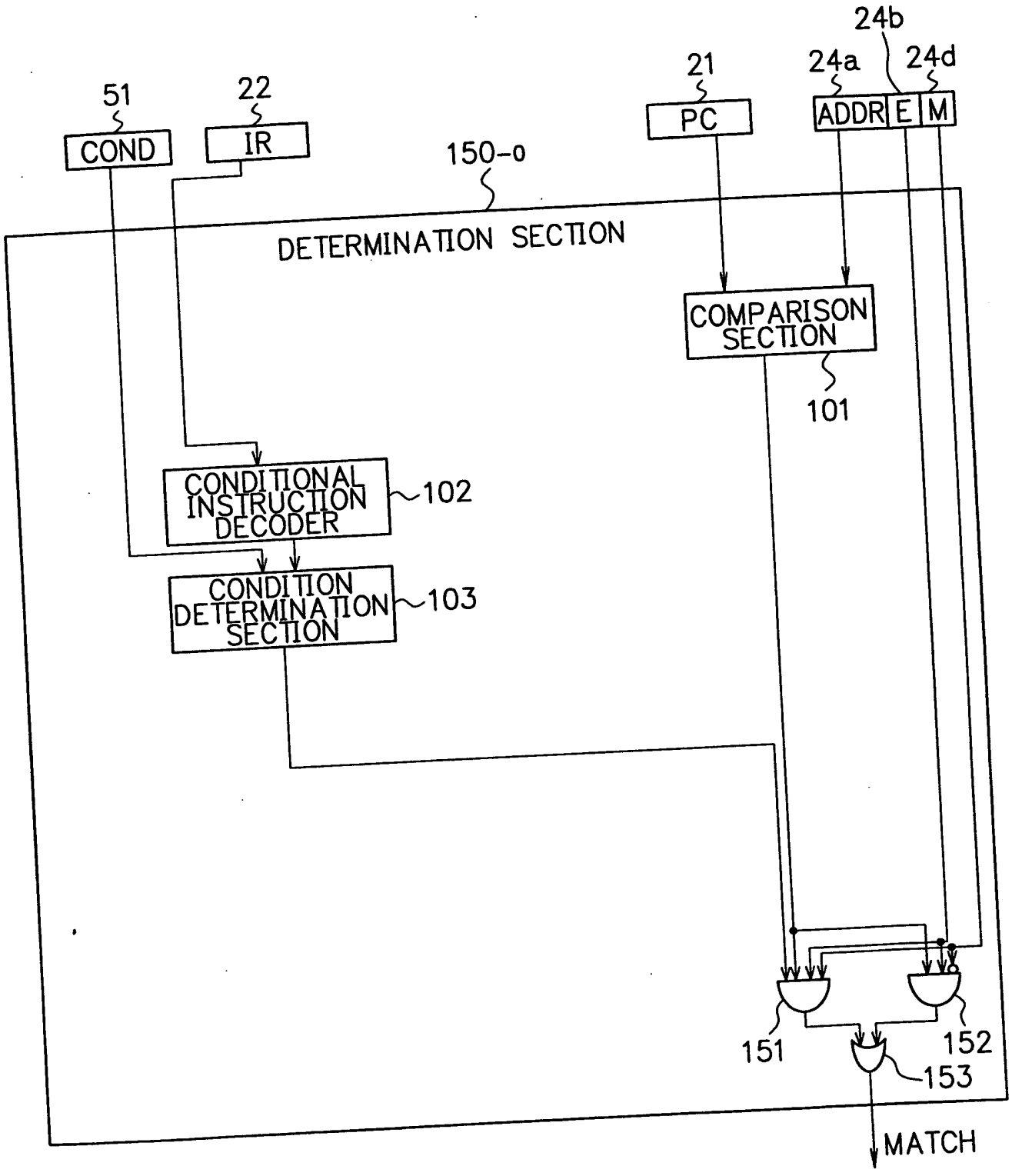
F I G. 27


51
COND
28
IR#0
IR#1
IR#i
21
PC
24c
24a
24b
ADDR
D
E
140-0
131
VALID INSTRUCTION ENCODER
COMPARISON SECTION
101
121
SELECTOR
SELECTOR
141
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
142
104
DETERMINATION SECTION
MATCH

F I G. 28


10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
150-0
DETERMINATION SECTION
MATCH
INTERRUPT
24a
24b
24d #0
ADDR
E
M
26
67
150-1
24-0
DETERMINATION SECTION
24d #1
150-2
24-1
DETERMINATION SECTION
24d #2
23
24-2
64,65
150-n
DETERMINATION SECTION
24d #n
24-n
MEMORY
INSTRUCTION FETCH
22
IR
62
30
50
REGISTER SECTION
DATA LOAD
COND
52
51
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
68
54
GR
55
70
DATA STORE
INTERRUPT
72
74
INTERRUPT CONTROL SECTION

F I G. 29


24b
21
24a
24d
51
22
PC
ADDR
E
M
COND
IR
150-o
DETERMINATION SECTION
COMPARISON SECTION
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
151
152
153
MATCH

F I G. 30

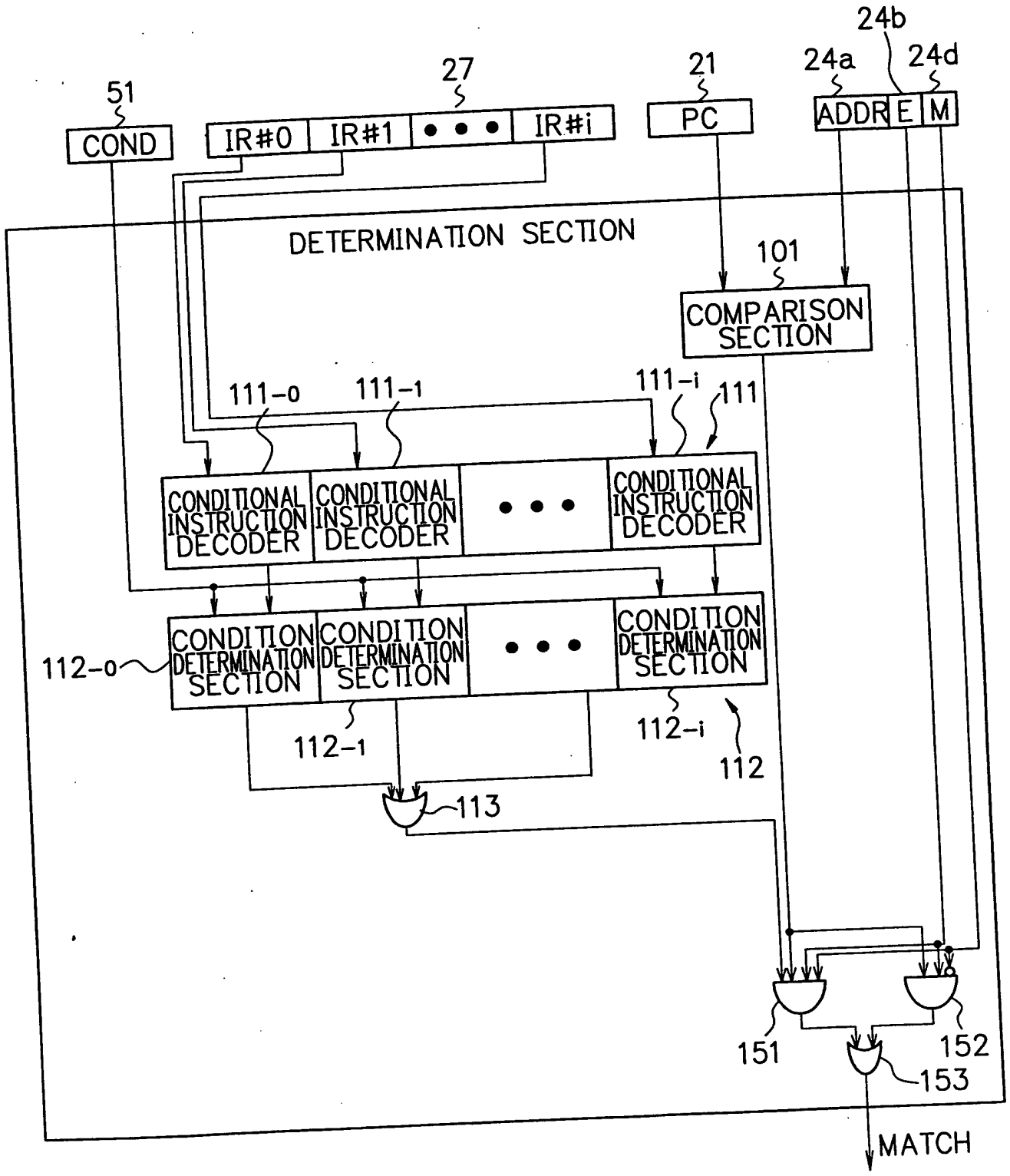

24b
24a
24d
27
21
51
ADDR
E
M
COND
IR#0
IR#1
IR#i
PC
DETERMINATION SECTION
101
COMPARISON SECTION
111-o
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
112-o
112-1
112-i
112
113
151
152
153
MATCH

FIG. 31

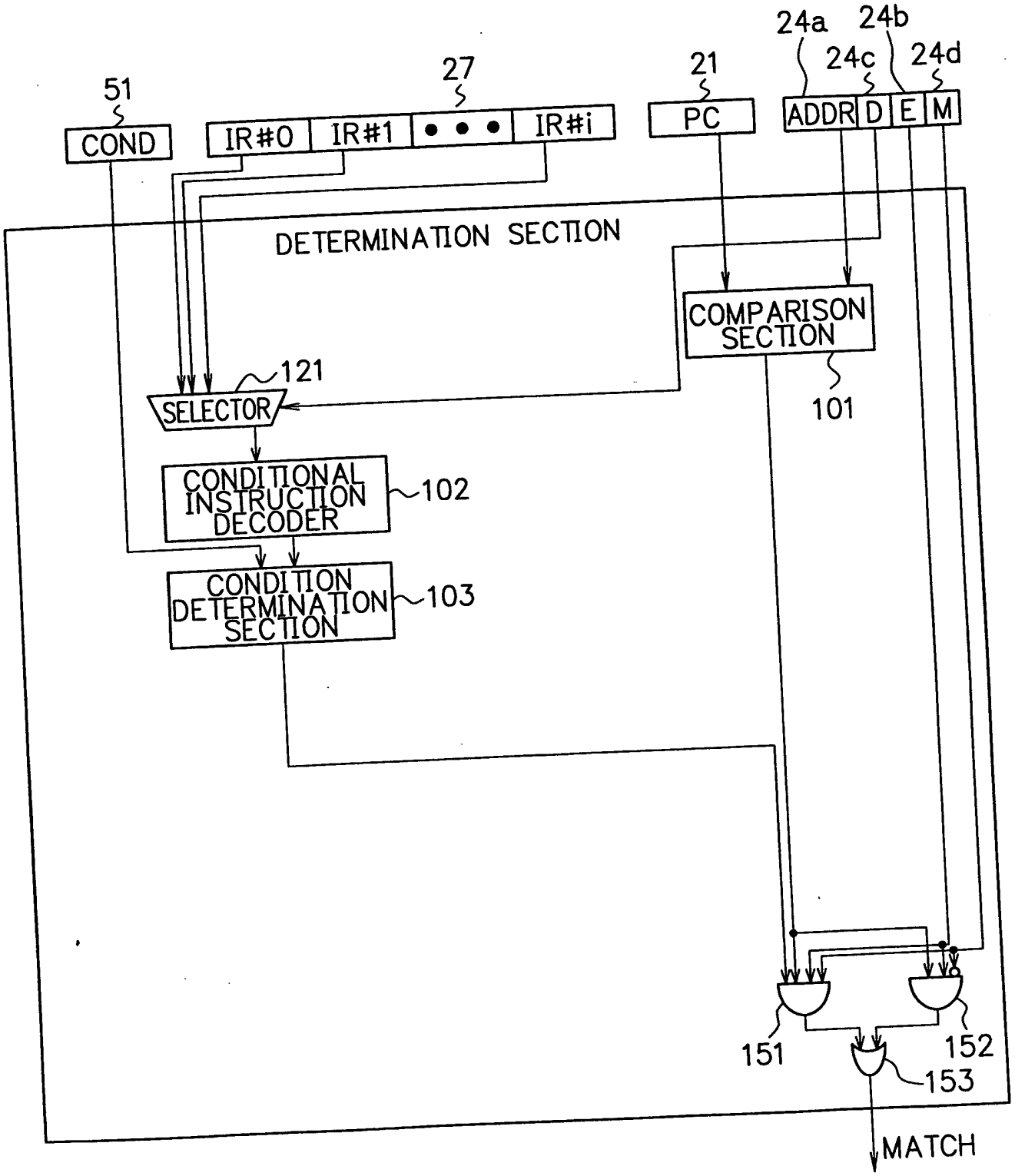

24a
24b
24c
24d
27
21
51
COND
IR#0
IR#1
IR#i
PC
ADDR
D
E
M
DETERMINATION SECTION
COMPARISON SECTION
101
121
SELECTOR
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
151
152
153
MATCH

FIG. 32

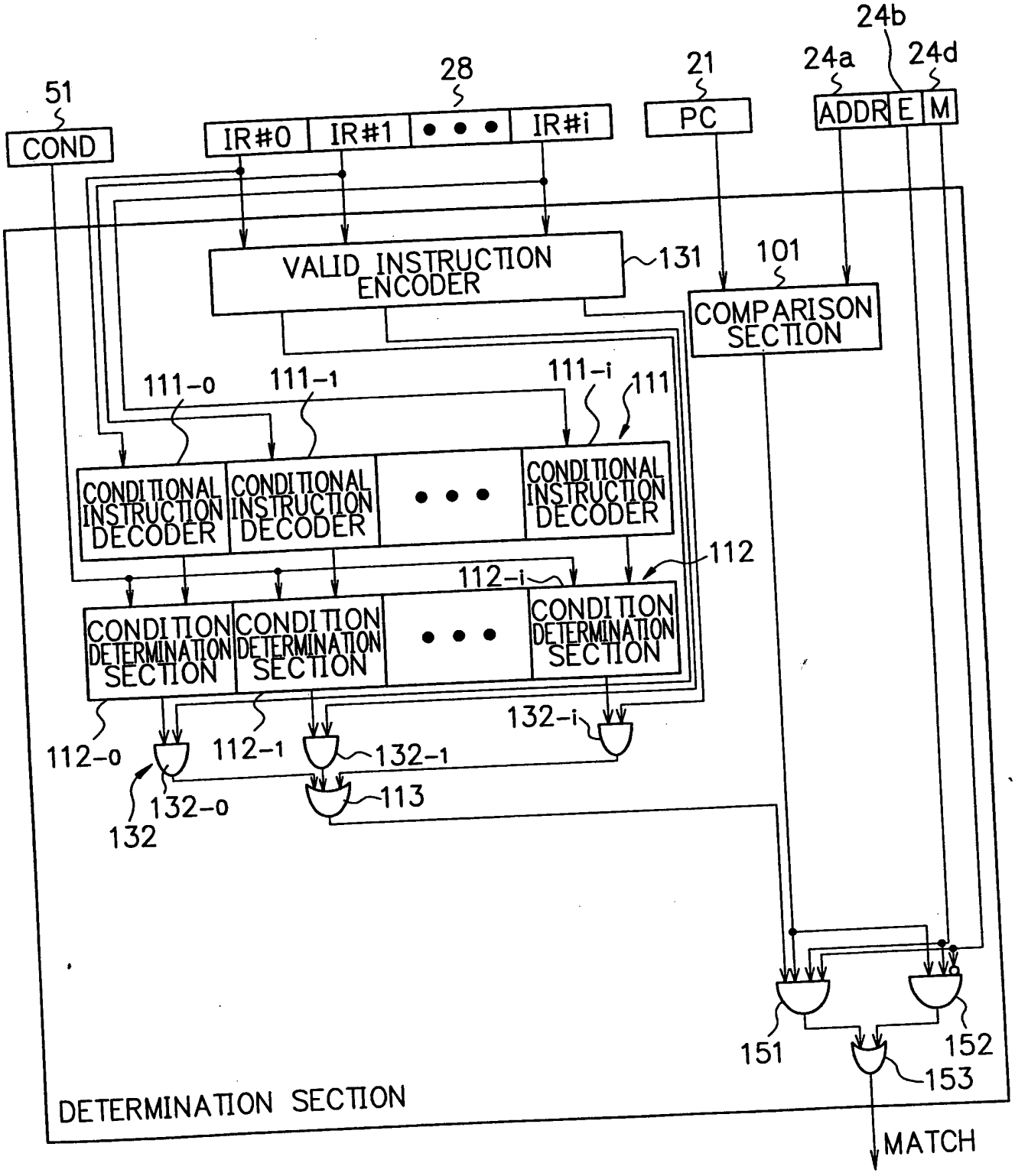

24b
24a
24d
28
21
51
ADDR
E
M
IR#0
IR#1
IR#i
PC
COND
VALID INSTRUCTION ENCODER
131
101
COMPARISON SECTION
111-o
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
112
112-i
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
112-o
112-1
132-i
132-1
132-o
132
113
151
152
153
DETERMINATION SECTION
MATCH

FIG. 33

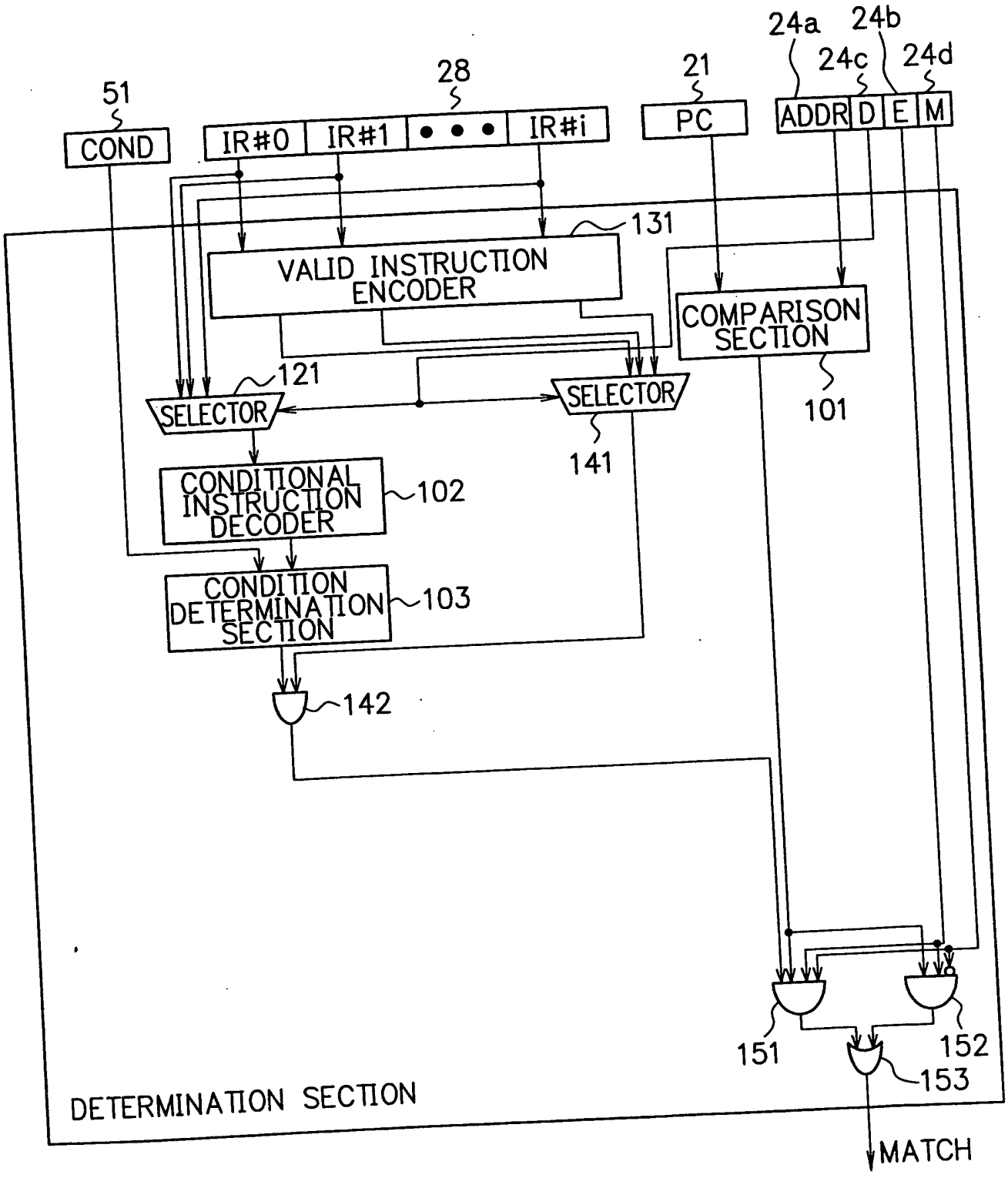

24a
24b
24c
24d
51
28
21
COND
IR#0
IR#1
IR#i
PC
ADDR
D
E
M
131
VALID INSTRUCTION ENCODER
COMPARISON SECTION
121
SELECTOR
SELECTOR
141
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
142
151
152
153
DETERMINATION SECTION
MATCH

FIG. 34

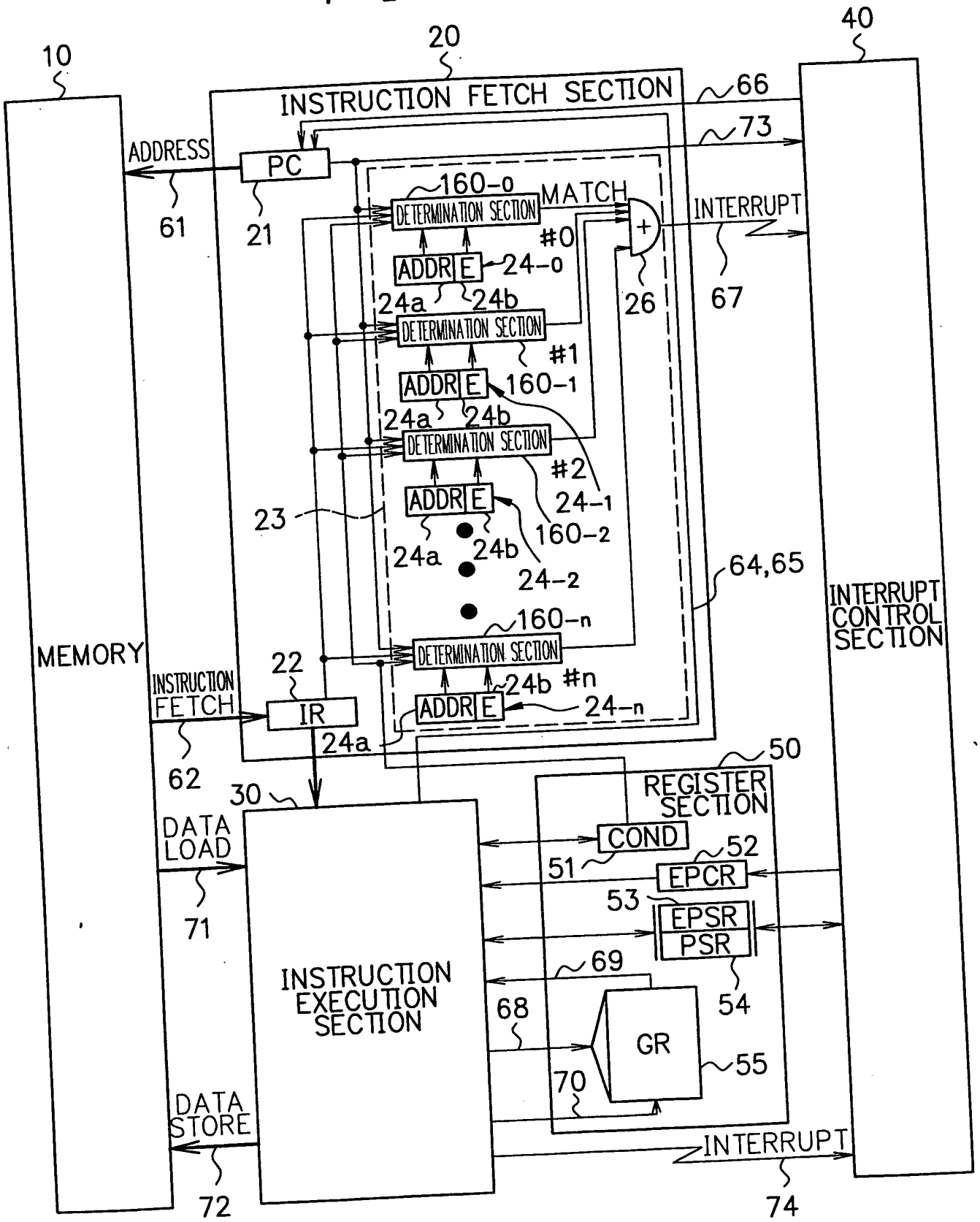
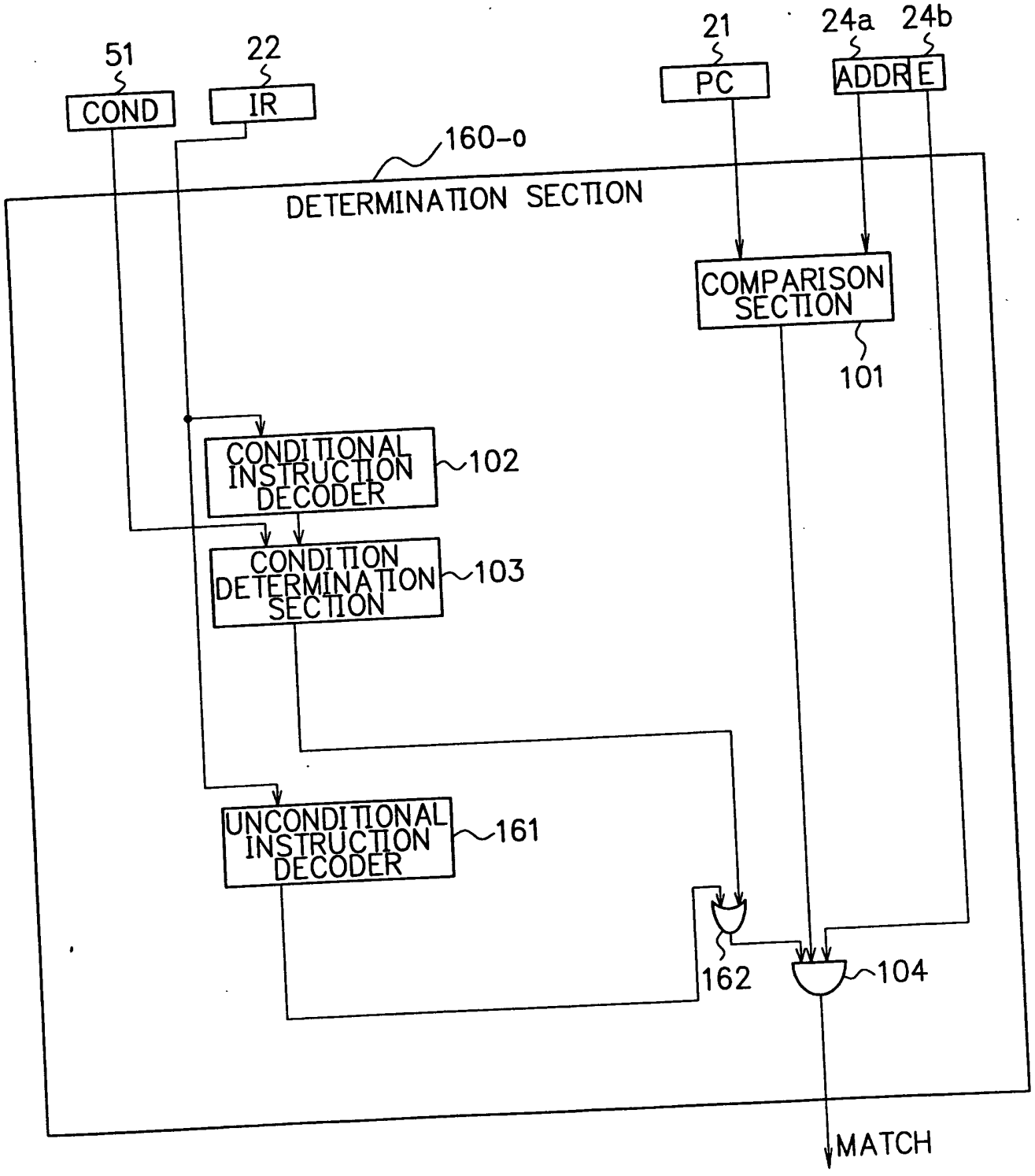

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
160-0
MATCH
DETERMINATION SECTION
#0
INTERRUPT
ADDR E
24-0
24a
24b
26
67
DETERMINATION SECTION
#1
ADDR E
160-1
24a
24b
DETERMINATION SECTION
#2
24-1
ADDR E
23
160-2
24a
24b
24-2
64,65
160-n
INTERRUPT CONTROL SECTION
MEMORY
DETERMINATION SECTION
22
INSTRUCTION FETCH
24b
#n
ADDR E
24-n
IR
24a
50
62
30
REGISTER SECTION
DATA LOAD
COND
51
52
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
54
68
GR
55
70
DATA STORE
INTERRUPT
72
74

FIG. 35


51
COND
22
IR
21
PC
24a
24b
ADDR
E
160-o
DETERMINATION SECTION
COMPARISON SECTION
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
UNCONDITIONAL INSTRUCTION DECODER
161
162
104
MATCH

F I G. 36

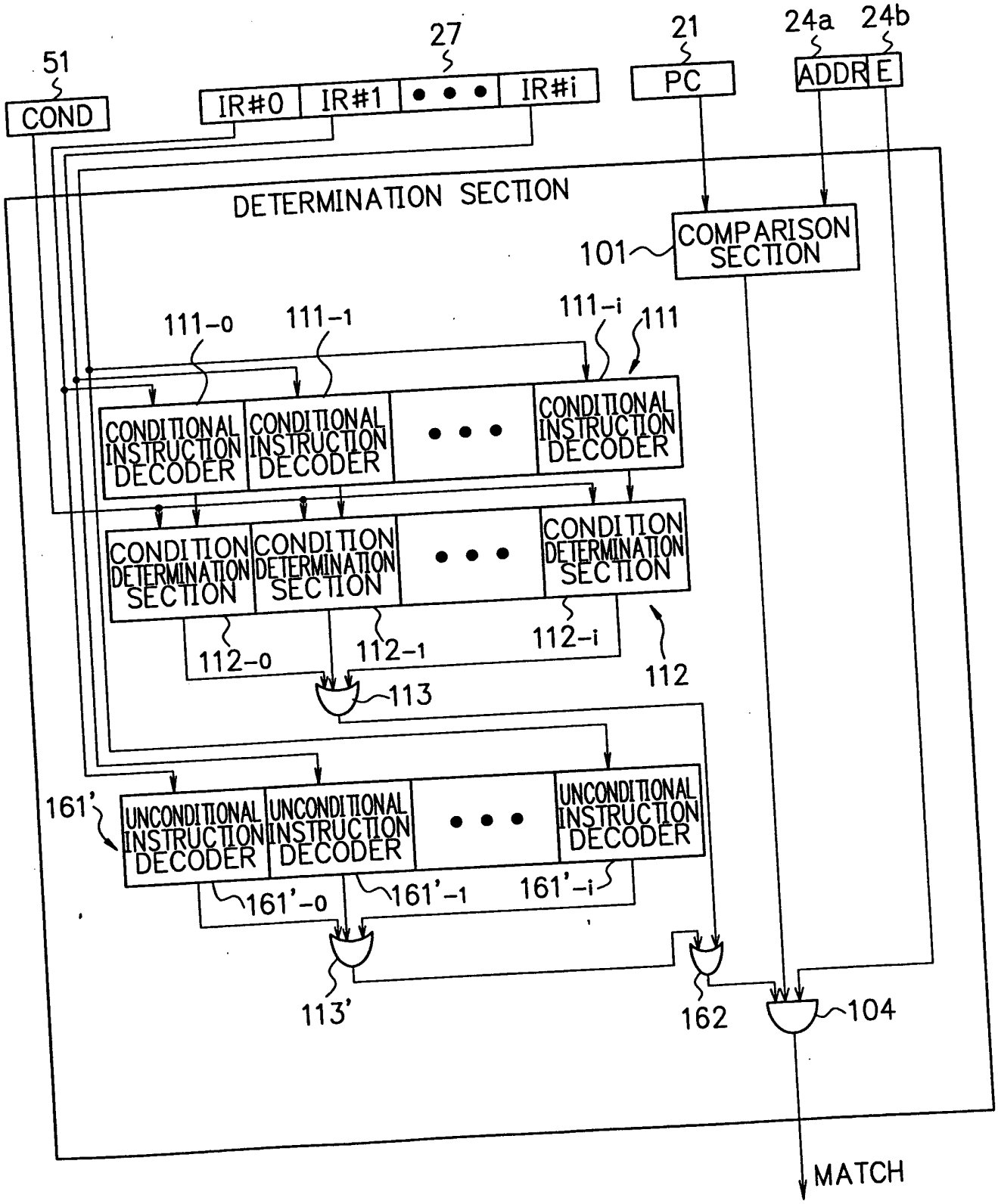

51
COND
27
IR#0
IR#1
IR#i
21
PC
24a
24b
ADDR
E
DETERMINATION SECTION
101
COMPARISON SECTION
111-0
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITION DETERMINATION SECTION
112-0
112-1
112-i
112
113
161'
UNCONDITIONAL INSTRUCTION DECODER
161'-0
161'-1
161'-i
113'
162
104
MATCH

FIG. 37

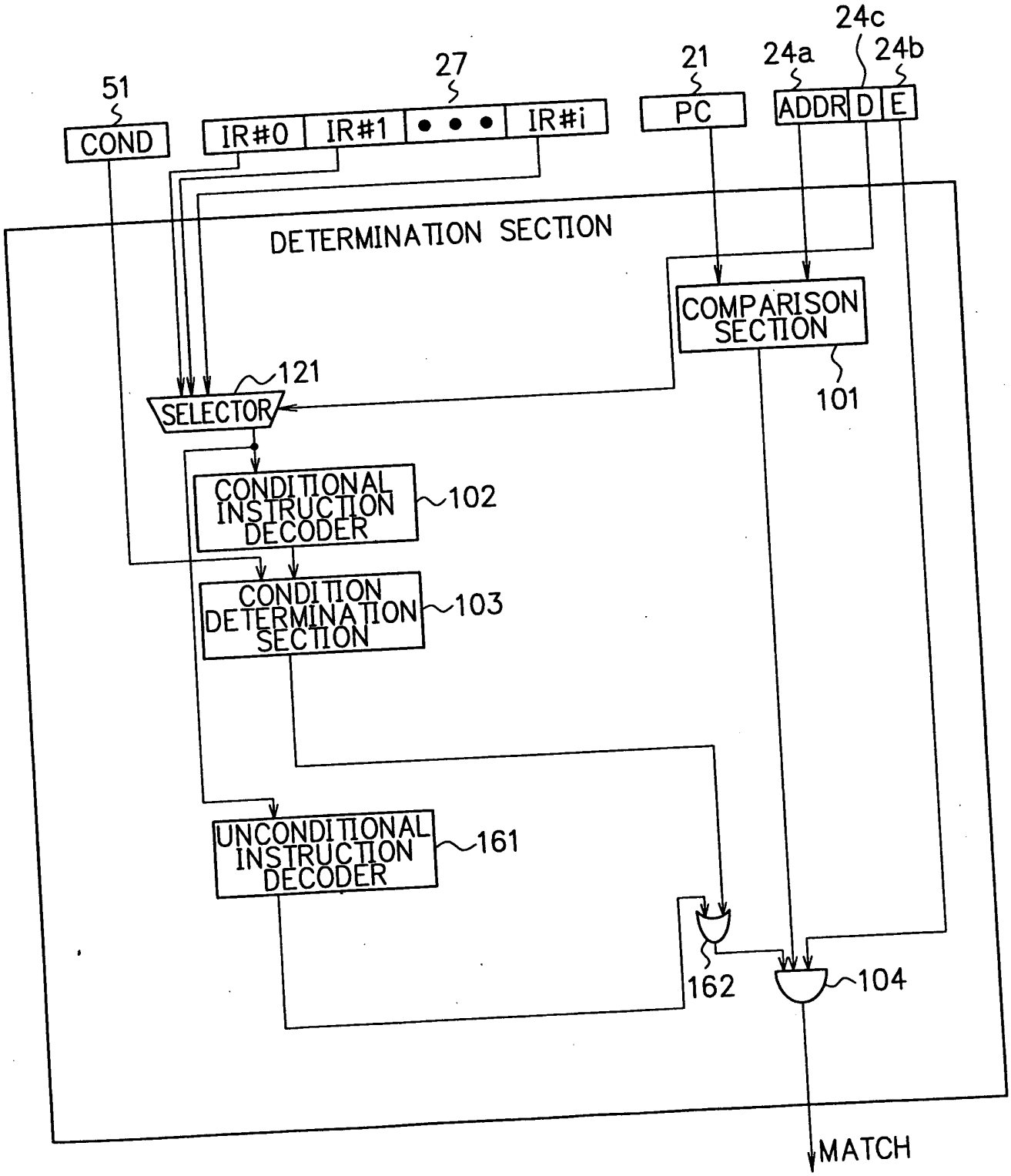

51
COND
27
IR#0
IR#1
IR#i
21
PC
24c
24a
24b
ADDR
D
E
DETERMINATION SECTION
COMPARISON SECTION
101
121
SELECTOR
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
UNCONDITIONAL INSTRUCTION DECODER
161
162
104
MATCH

FIG. 38

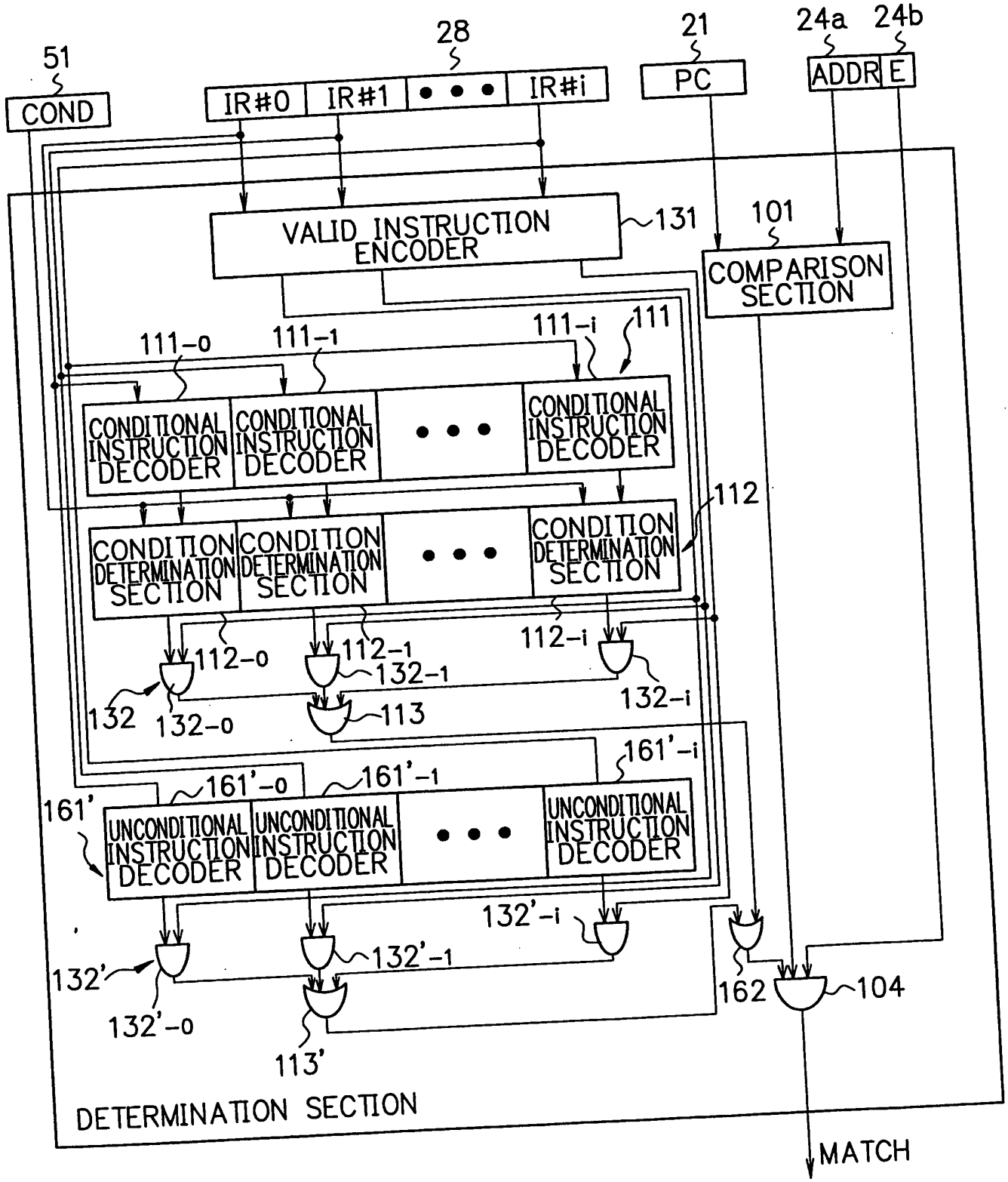
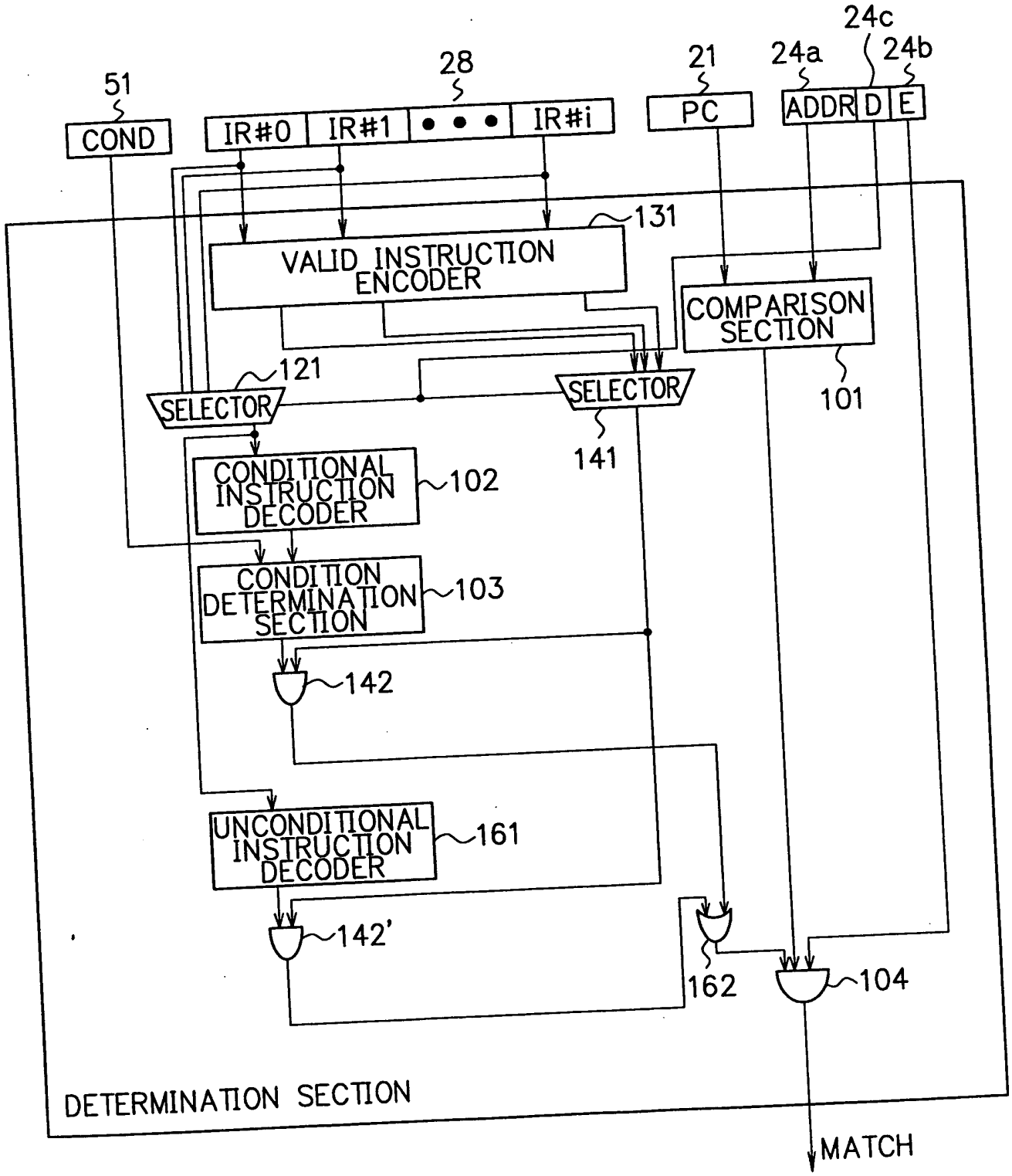

51
COND
28
IR#0
IR#1
IR#i
21
PC
24a
24b
ADDR
E
VALID INSTRUCTION ENCODER
131
101
COMPARISON SECTION
111-0
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITION DETERMINATION SECTION
112
112-0
112-1
112-i
132-1
132-i
132
132-0
113
161'-i
161'-0
161'-1
161'
UNCONDITIONAL INSTRUCTION DECODER
132'-i
132'-1
132'
132'-0
162
104
113'
DETERMINATION SECTION
MATCH

FIG. 39


51
COND
28
IR#0
IR#1
IR#i
21
PC
24a
24c
24b
ADDR
D
E
131
VALID INSTRUCTION ENCODER
COMPARISON SECTION
101
121
SELECTOR
SELECTOR
141
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
142
UNCONDITIONAL INSTRUCTION DECODER
161
142'
162
104
DETERMINATION SECTION
MATCH

F I G. 40

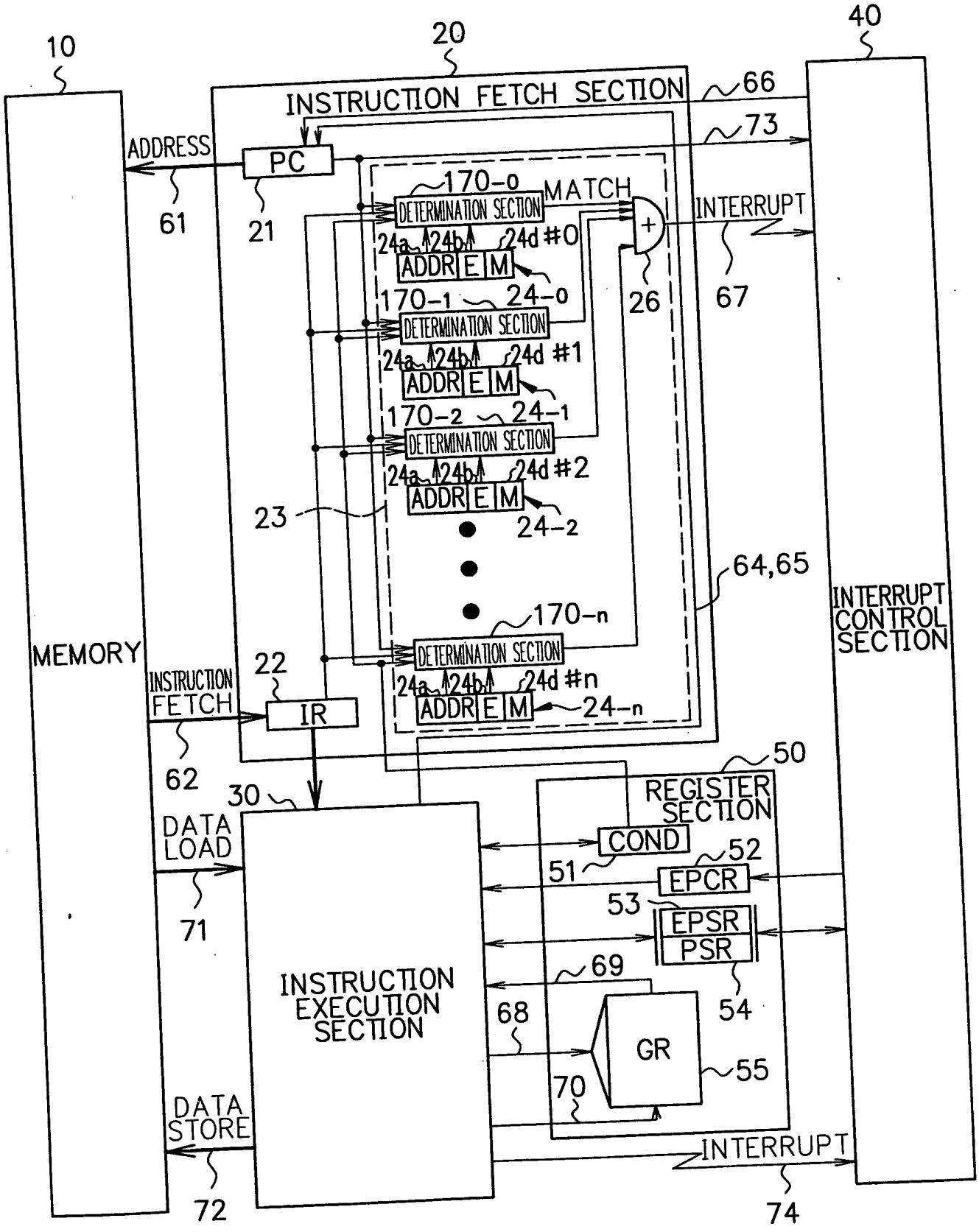

10
20
40
INSTRUCTION FETCH SECTION
66
73
ADDRESS
PC
61
21
170-o
MATCH
DETERMINATION SECTION
INTERRUPT
24a
24b
24d #0
ADDR
E
M
26
67
170-1
24-o
DETERMINATION SECTION
24d #1
170-2
24-1
DETERMINATION SECTION
24d #2
23
24-2
64,65
INTERRUPT CONTROL SECTION
170-n
MEMORY
22
DETERMINATION SECTION
24d #n
INSTRUCTION FETCH
IR
24-n
62
30
50
REGISTER SECTION
DATA LOAD
COND
51
52
EPCR
53
EPSR
PSR
71
INSTRUCTION EXECUTION SECTION
69
68
54
GR
55
70
DATA STORE
INTERRUPT
72
74

FIG. 41

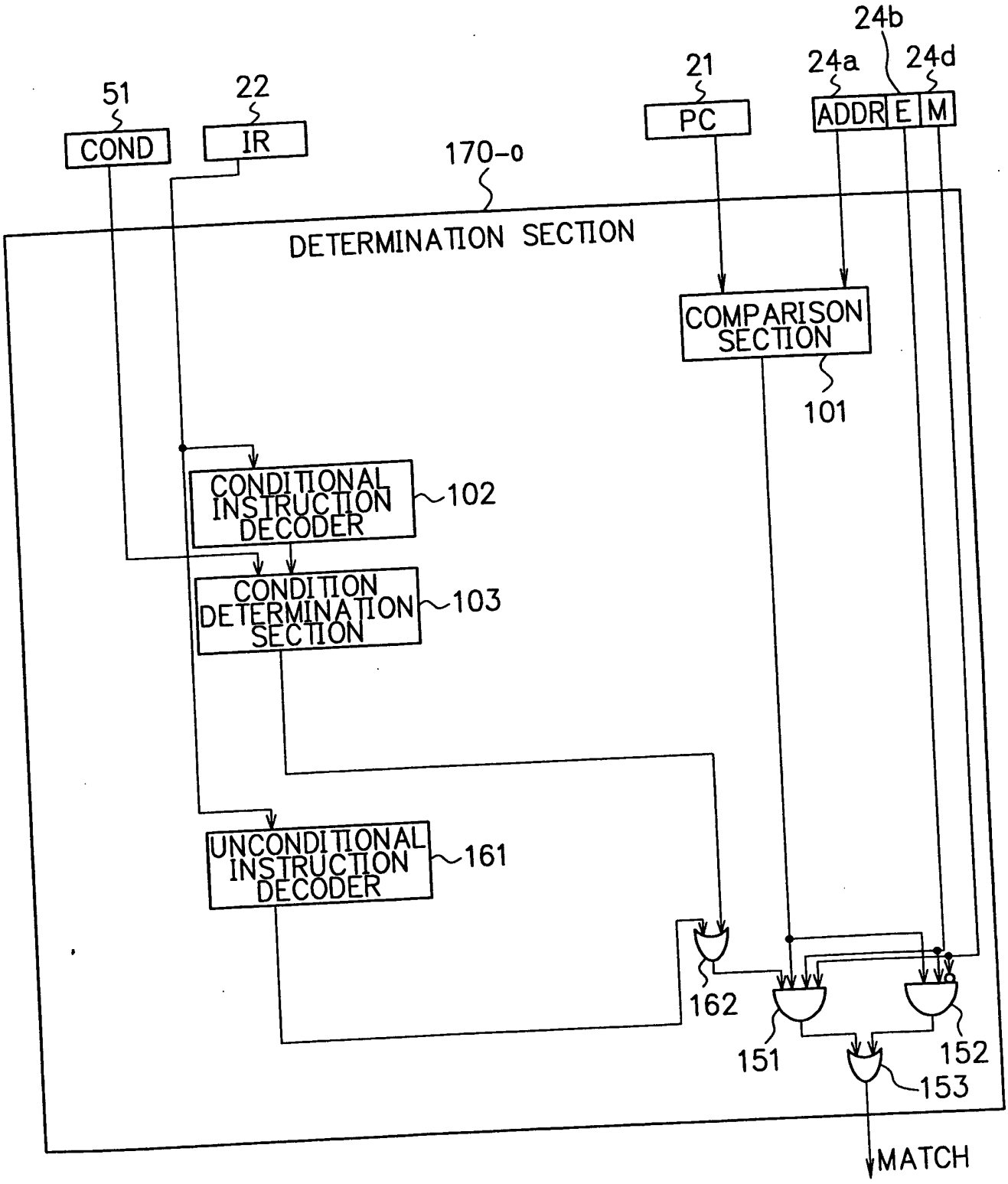

24b
21
24a
24d
51
22
PC
ADDR
E
M
COND
IR
170-o
DETERMINATION SECTION
COMPARISON SECTION
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
UNCONDITIONAL INSTRUCTION DECODER
161
162
151
152
153
MATCH

FIG. 42

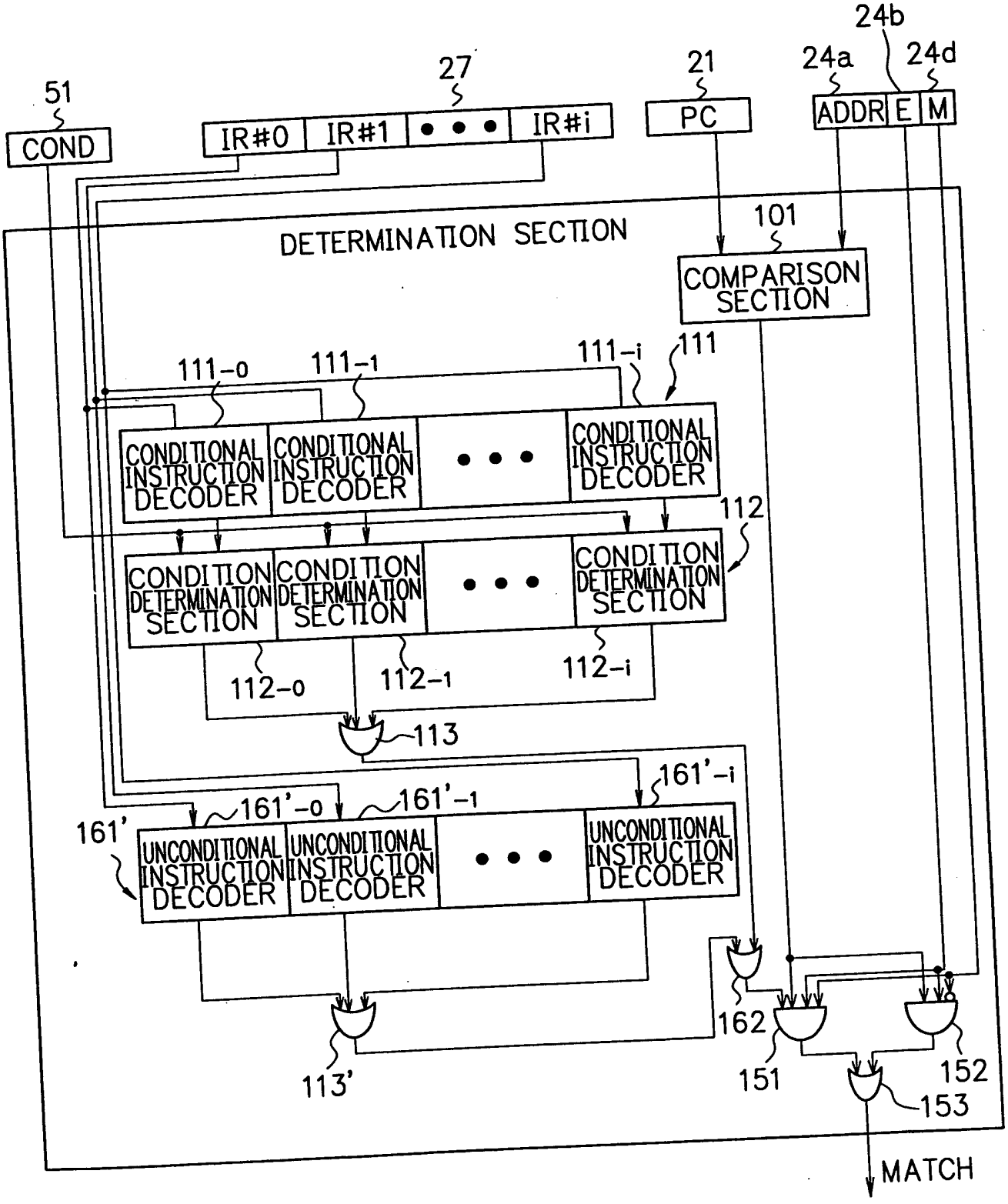

24b
24a
24d
27
21
51
ADDR
E
M
PC
COND
IR#0
IR#1
IR#i
DETERMINATION SECTION
101
COMPARISON SECTION
111-o
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
CONDITIONAL INSTRUCTION DECODER
112
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
CONDITION DETERMINATION SECTION
112-o
112-1
112-i
113
161'-i
161'-o
161'-1
161'
UNCONDITIONAL INSTRUCTION DECODER
UNCONDITIONAL INSTRUCTION DECODER
UNCONDITIONAL INSTRUCTION DECODER
162
151
152
153
113'
MATCH

FIG. 43

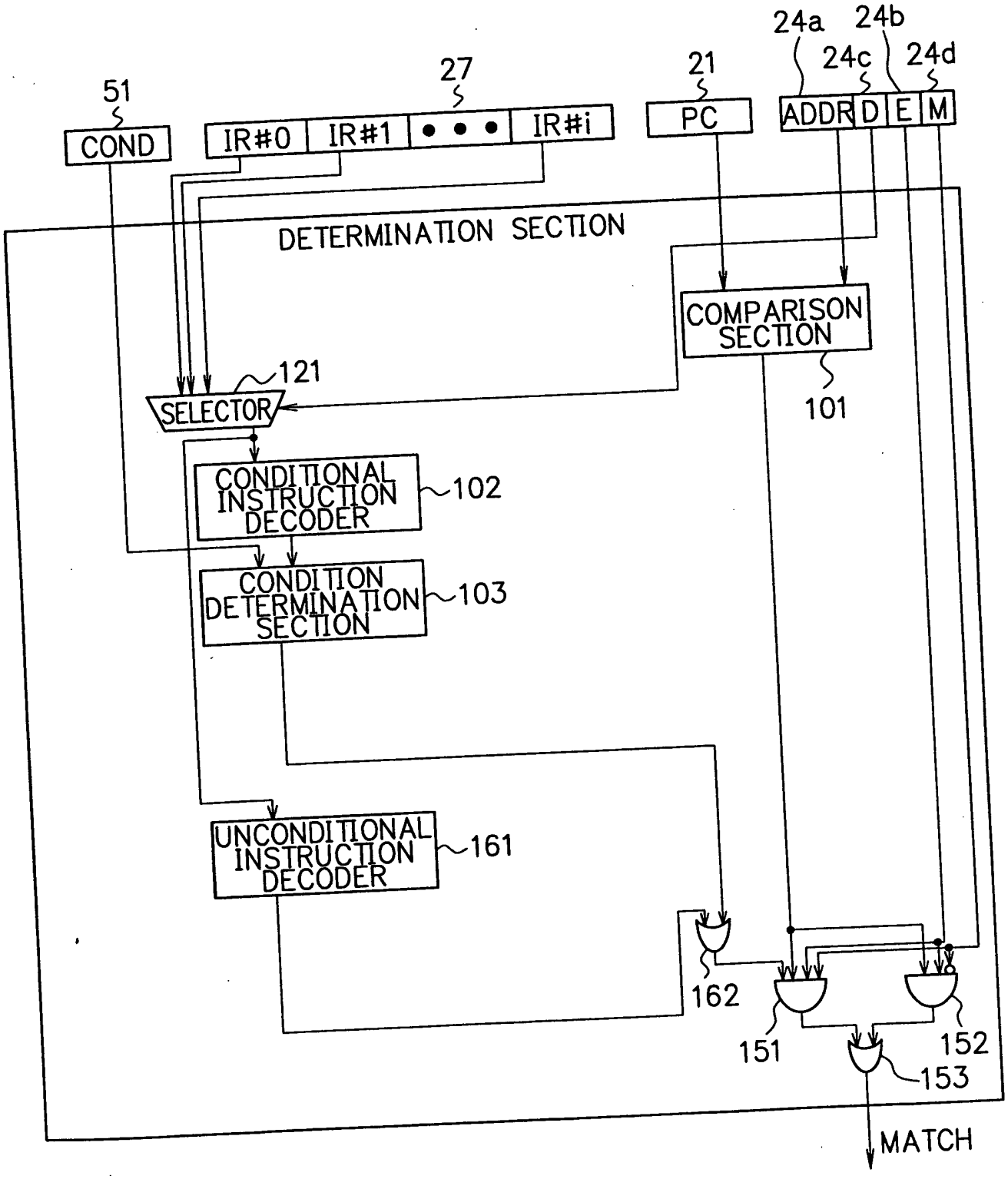

24a
24b
24c
24d
51
27
21
COND
IR#0
IR#1
IR#i
PC
ADDR
D
E
M
DETERMINATION SECTION
COMPARISON SECTION
101
121
SELECTOR
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
UNCONDITIONAL INSTRUCTION DECODER
161
162
151
152
153
MATCH

FIG. 44

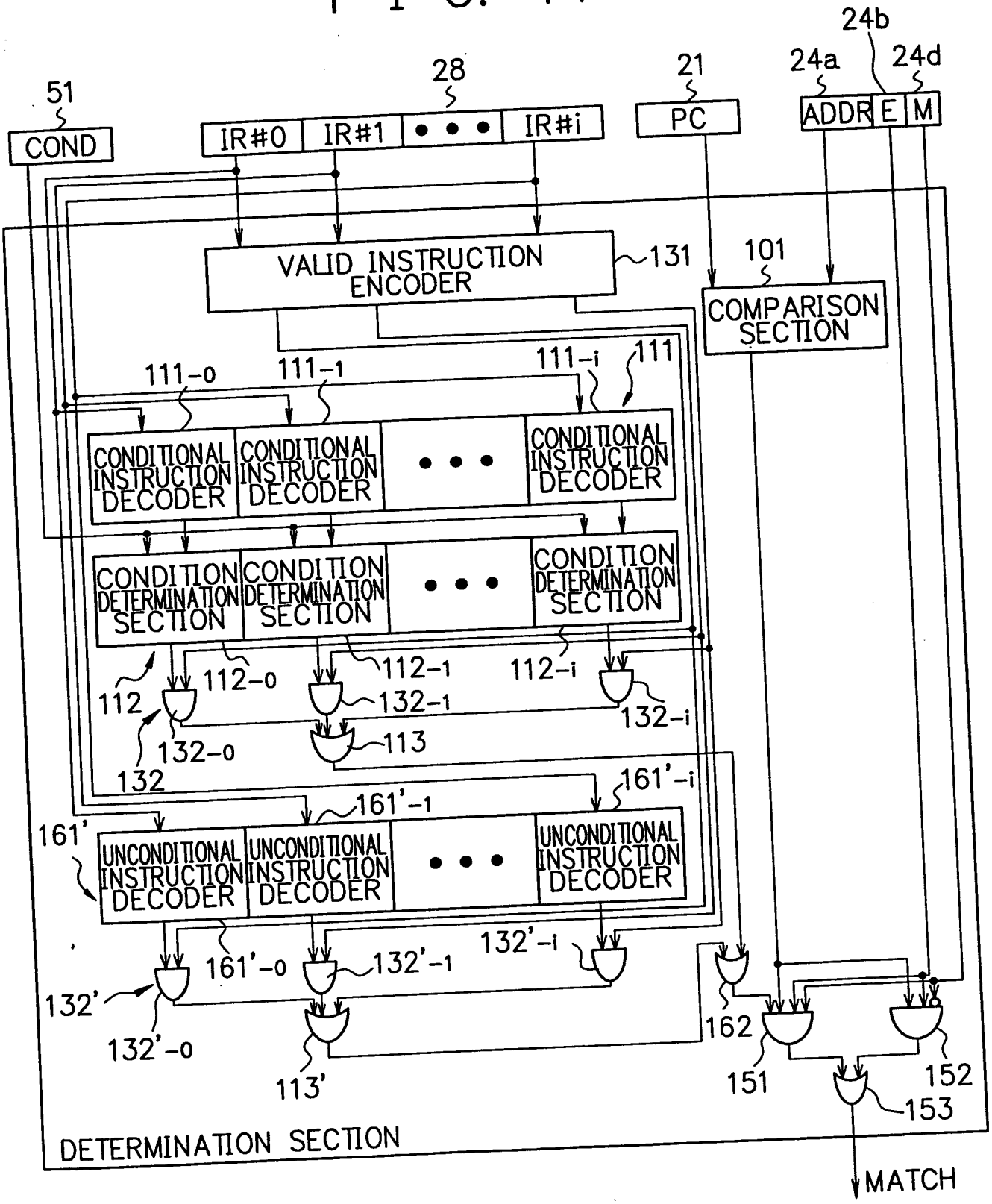

51
COND
28
IR#0
IR#1
IR#i
21
PC
24b
24a
24d
ADDR
E
M
VALID INSTRUCTION ENCODER
131
101
COMPARISON SECTION
111-0
111-1
111-i
111
CONDITIONAL INSTRUCTION DECODER
CONDITION DETERMINATION SECTION
112
112-0
112-1
112-i
132-0
132-1
132-i
132
113
161'
161'-1
161'-i
UNCONDITIONAL INSTRUCTION DECODER
161'-0
132'
132'-0
132'-1
132'-i
113'
162
151
152
153
DETERMINATION SECTION
MATCH

FIG. 45

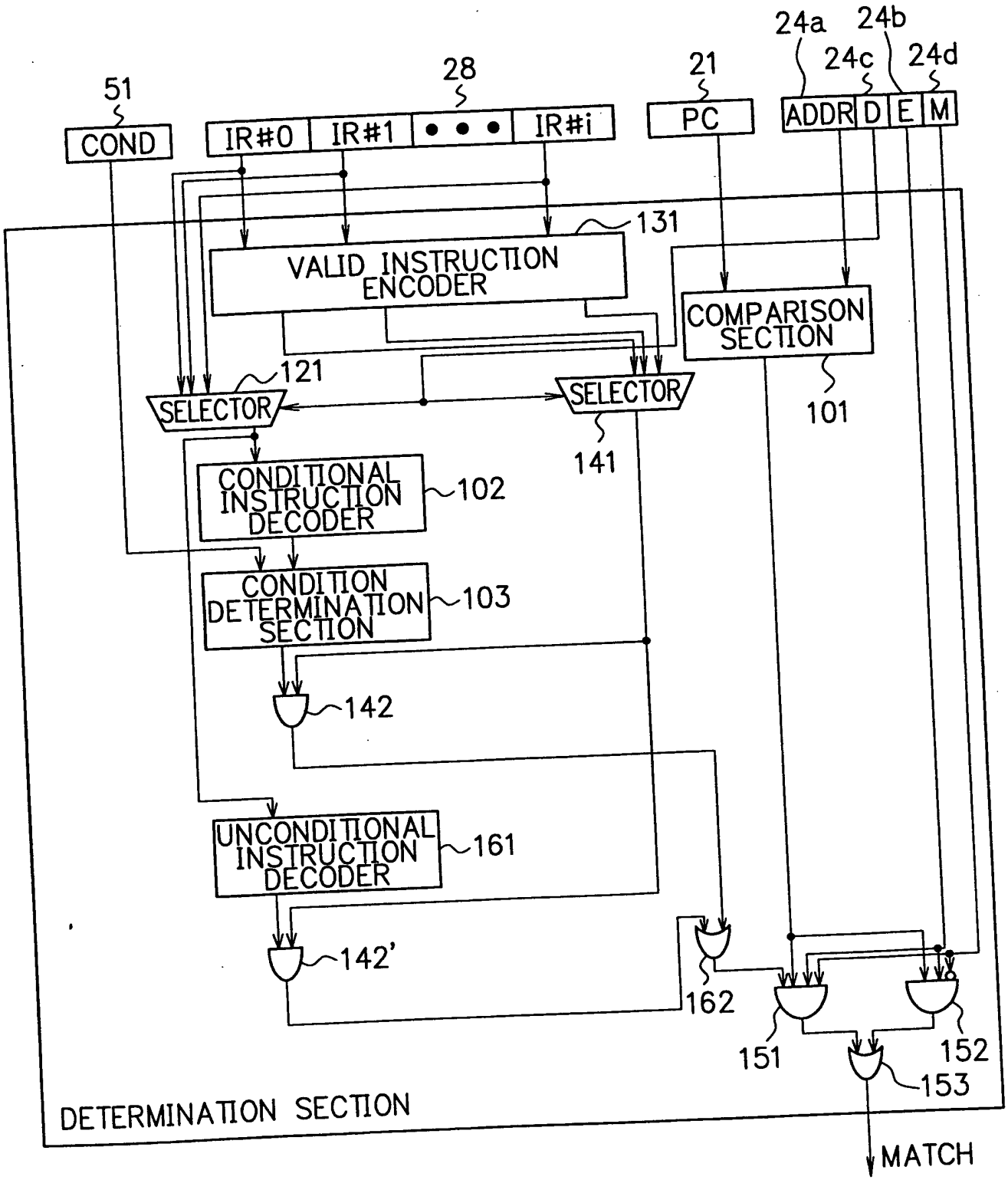

24a
24b
24c
24d
51
28
21
COND
IR#0
IR#1
IR#i
PC
ADDR
D
E
M
131
VALID INSTRUCTION ENCODER
COMPARISON SECTION
121
SELECTOR
SELECTOR
141
101
CONDITIONAL INSTRUCTION DECODER
102
CONDITION DETERMINATION SECTION
103
142
UNCONDITIONAL INSTRUCTION DECODER
161
142'
162
151
152
153
DETERMINATION SECTION
MATCH

FIG. 46

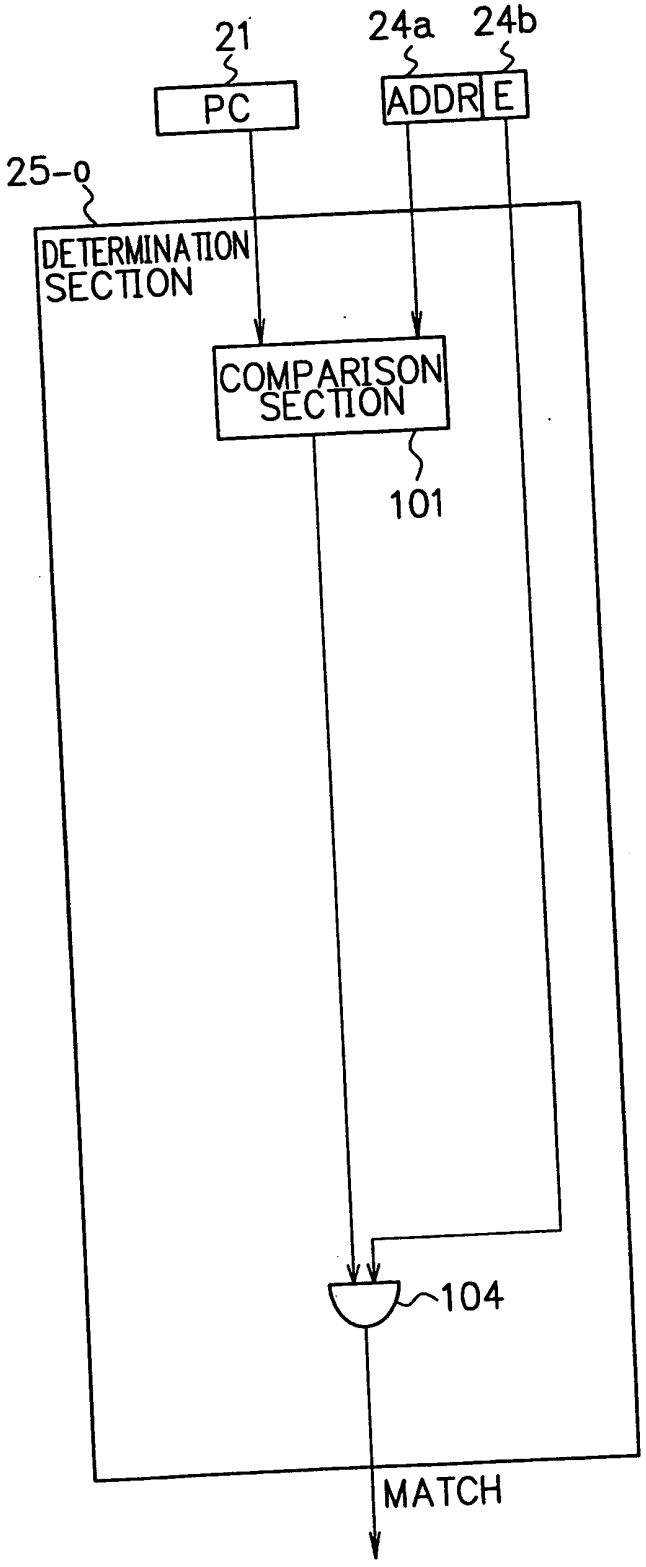

21
24a
24b
PC
ADDR
E
25-o
DETERMINATION SECTION
COMPARISON SECTION
101
104
MATCH

FIG. 47

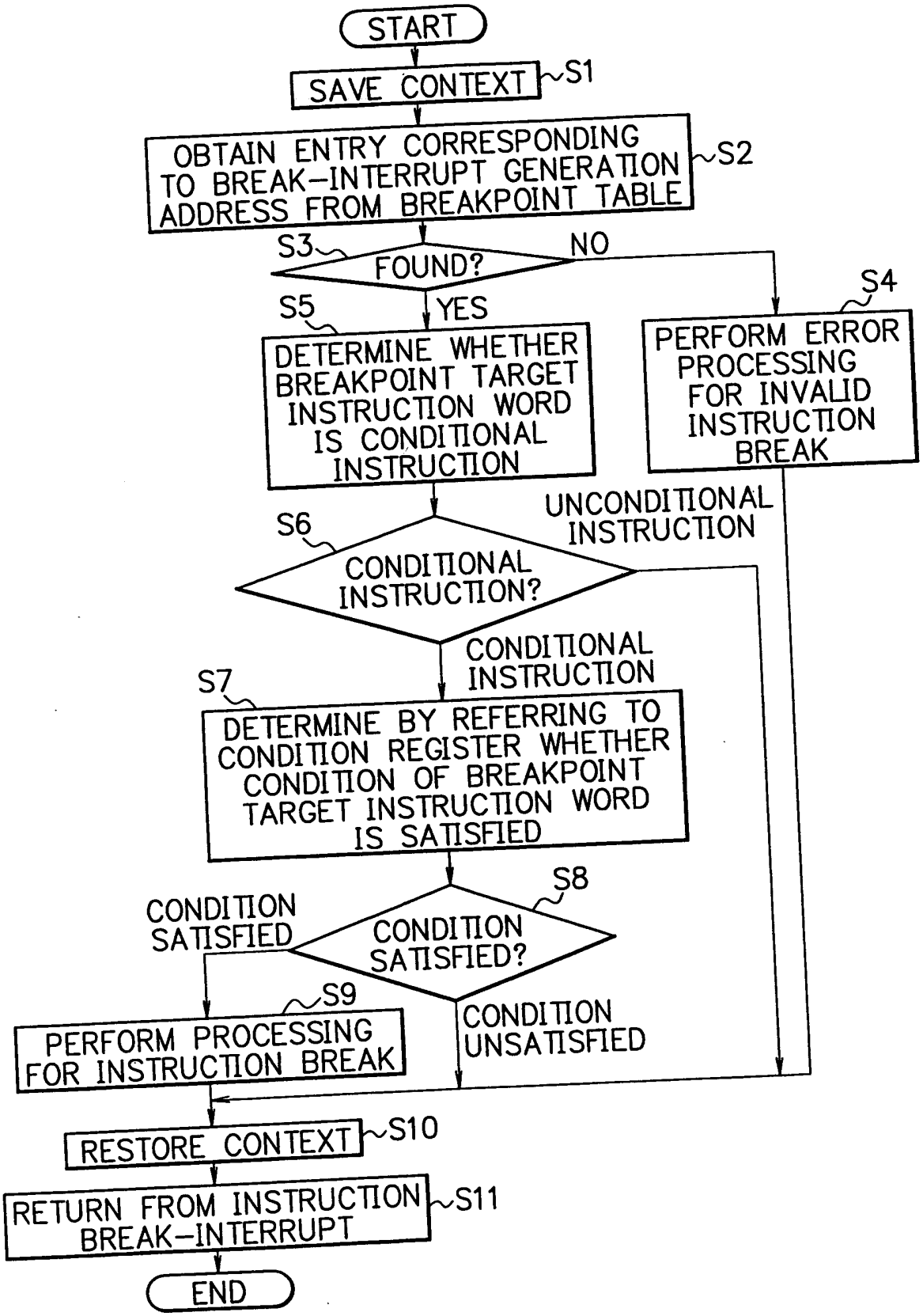

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S5
DETERMINE WHETHER BREAKPOINT TARGET INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
S6
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S7
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED?
CONDITION SATISFIED
CONDITION UNSATISFIED
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 48

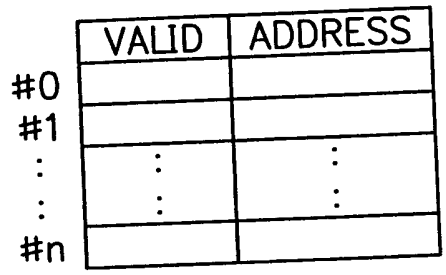


FIG. 49

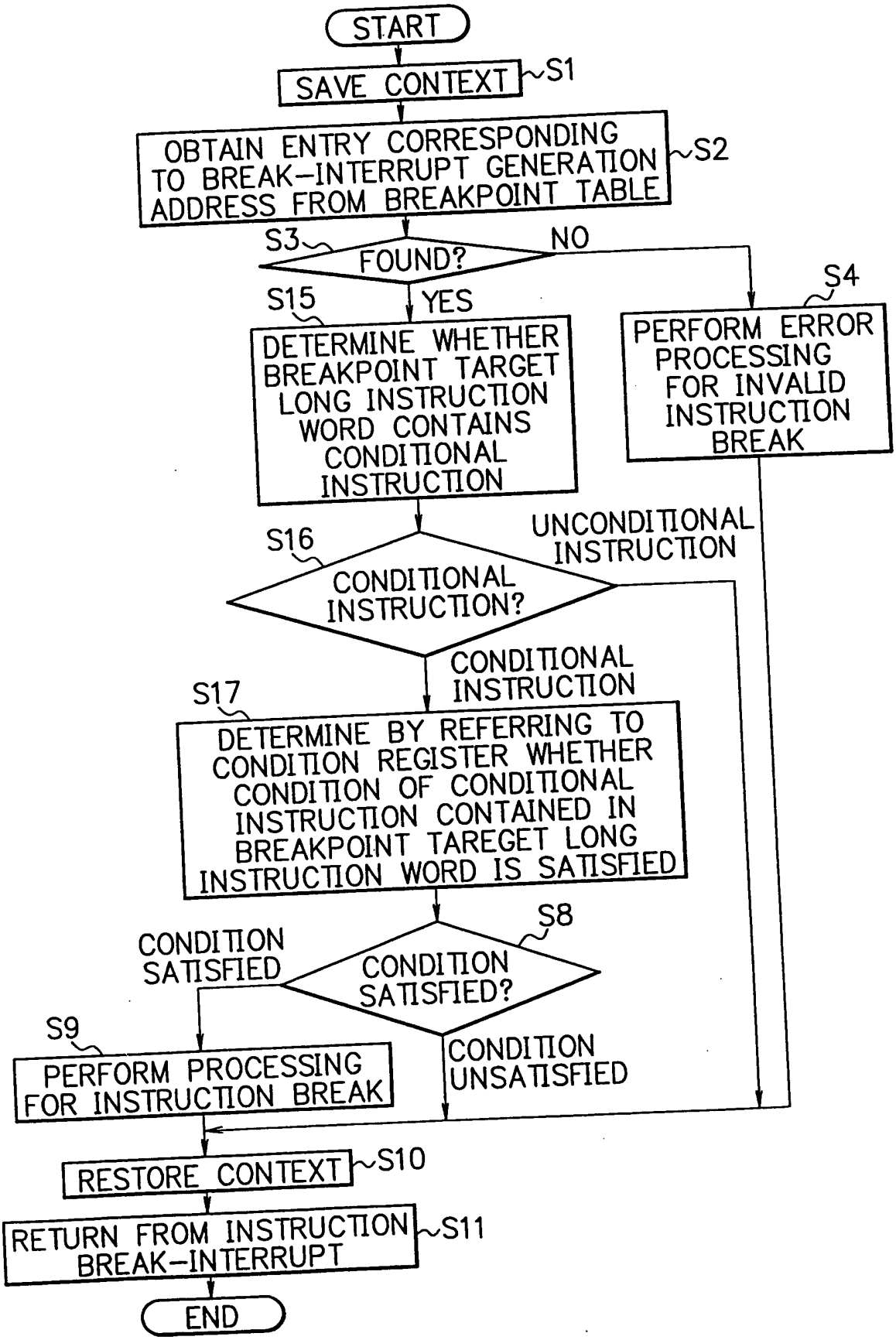

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S15
DETERMINE WHETHER BREAKPOINT TARGET LONG INSTRUCTION WORD CONTAINS CONDITIONAL INSTRUCTION
S16
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S17
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF CONDITIONAL INSTRUCTION CONTAINED IN BREAKPOINT TAREGET LONG INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED?
CONDITION SATISFIED
CONDITION UNSATISFIED
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 50

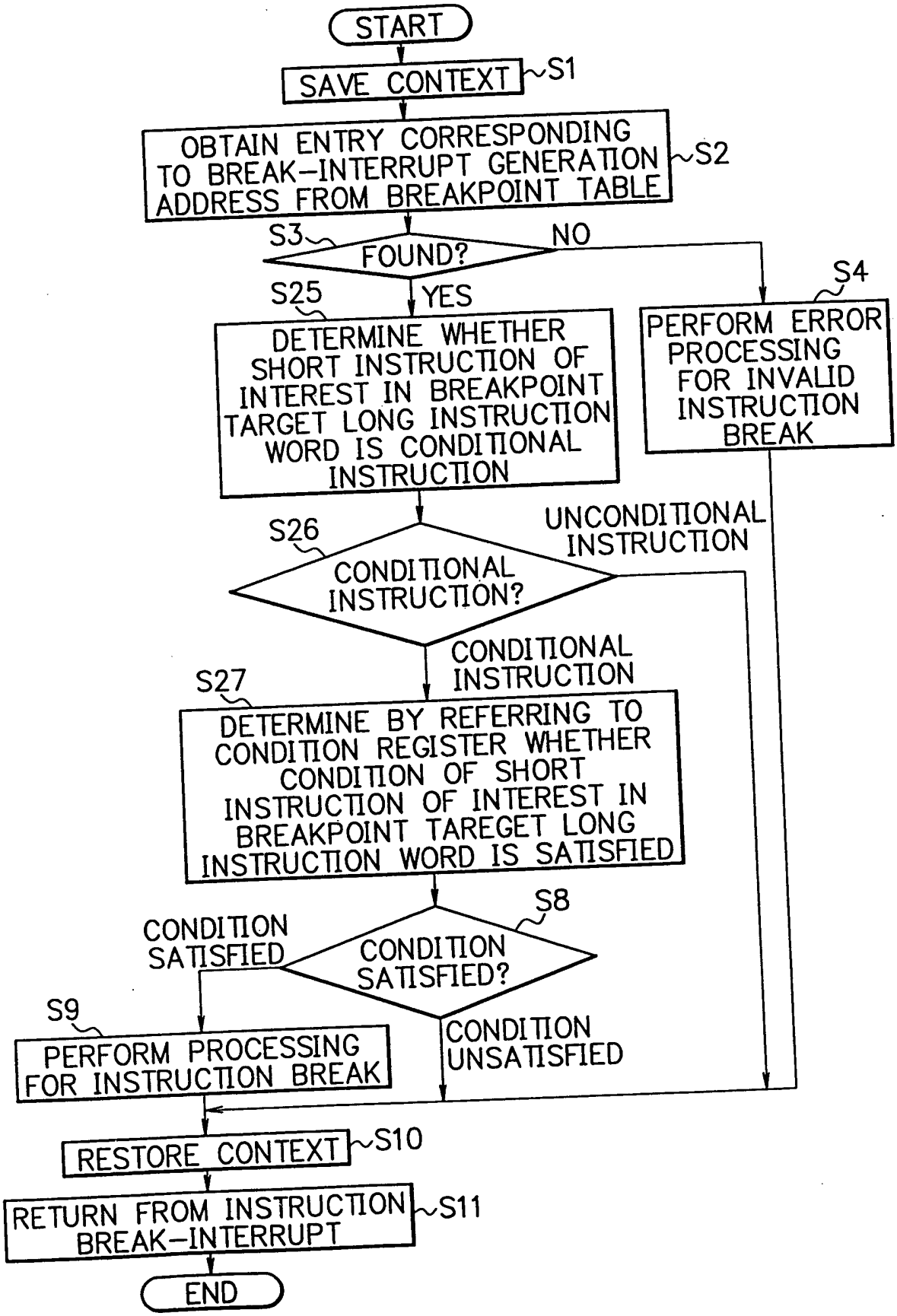

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S25
DETERMINE WHETHER SHORT INSTRUCTION OF INTEREST IN BREAKPOINT TARGET LONG INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
S26
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S27
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF SHORT INSTRUCTION OF INTEREST IN BREAKPOINT TAREGET LONG INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED?
CONDITION SATISFIED
CONDITION UNSATISFIED
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 51

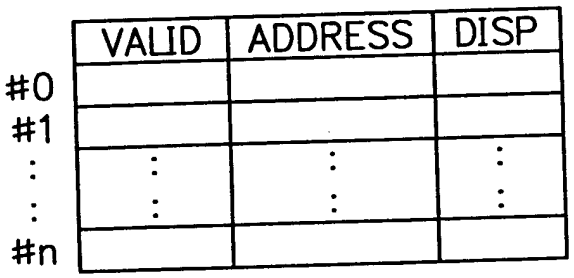


FIG. 52

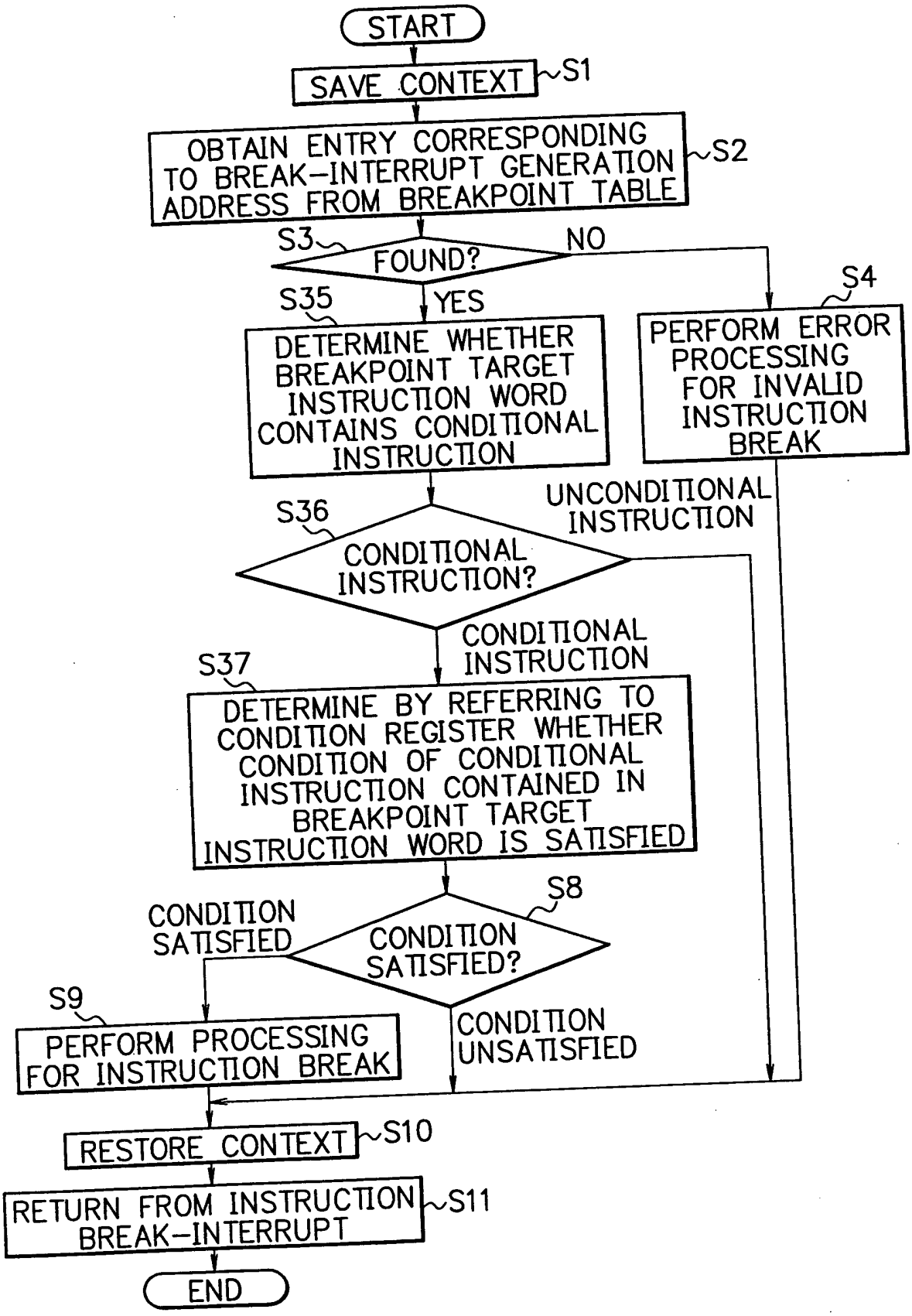

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S35
DETERMINE WHETHER BREAKPOINT TARGET INSTRUCTION WORD CONTAINS CONDITIONAL INSTRUCTION
S36
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S37
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF CONDITIONAL INSTRUCTION CONTAINED IN BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED?
CONDITION SATISFIED
CONDITION UNSATISFIED
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 53

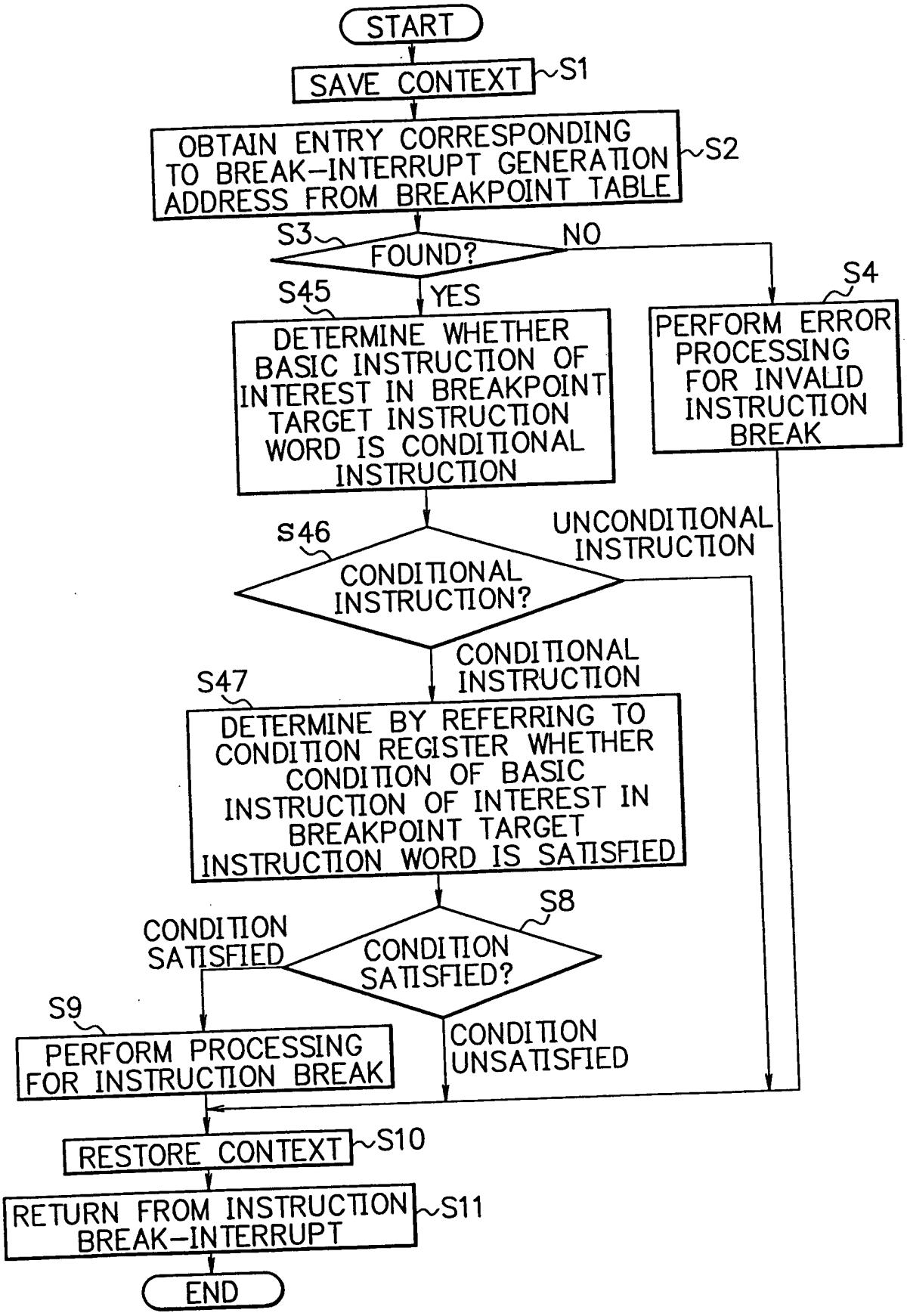

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S45
DETERMINE WHETHER BASIC INSTRUCTION OF INTEREST IN BREAKPOINT TARGET INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
S46
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S47
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF BASIC INSTRUCTION OF INTEREST IN BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED?
CONDITION SATISFIED
CONDITION UNSATISFIED
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 54

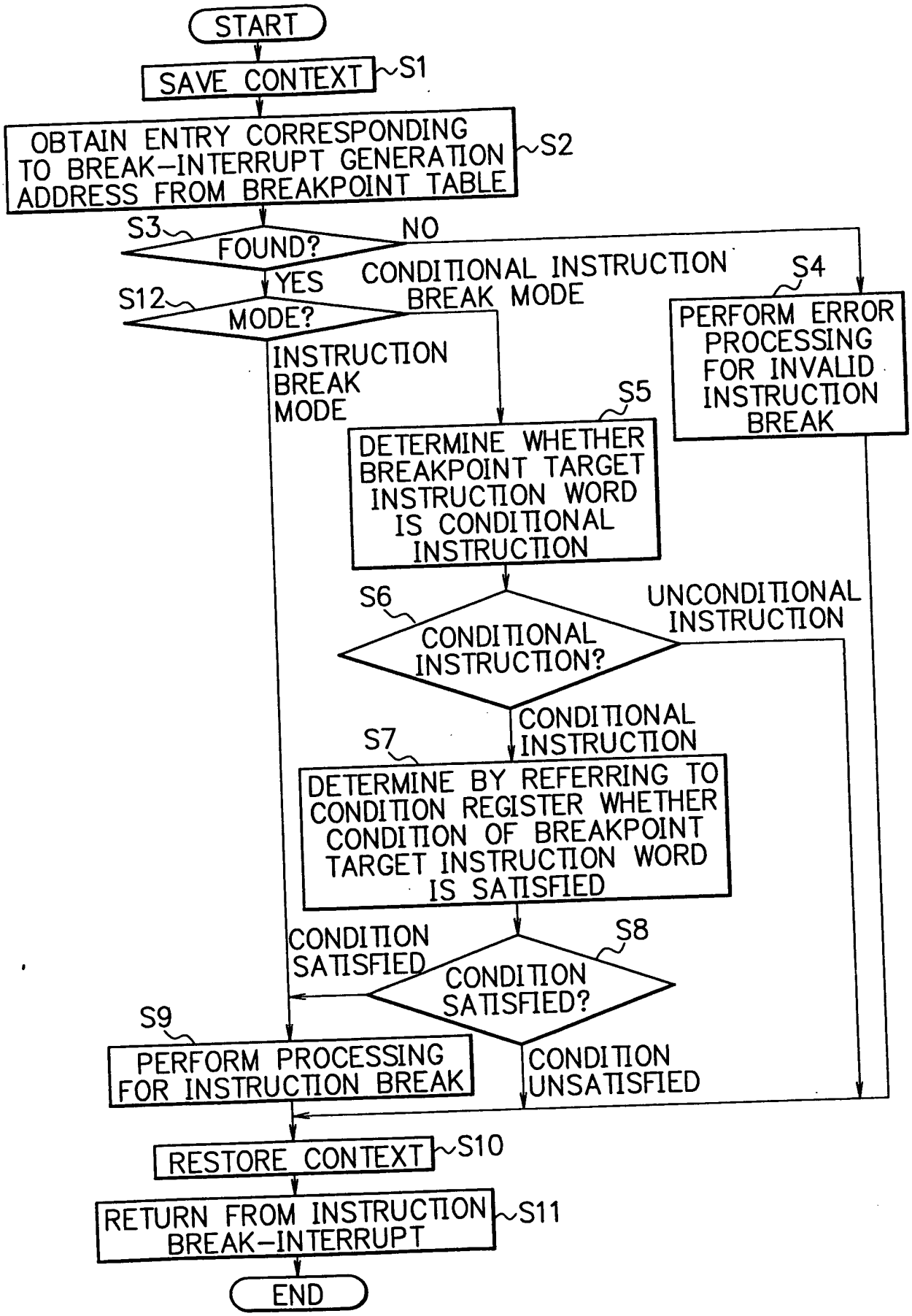

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
CONDITIONAL INSTRUCTION BREAK MODE
S4
S12
MODE?
INSTRUCTION BREAK MODE
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S5
DETERMINE WHETHER BREAKPOINT TARGET INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
S6
CONDITIONAL INSTRUCTION?
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION
S7
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
CONDITION SATISFIED
S8
CONDITION SATISFIED?
S9
PERFORM PROCESSING FOR INSTRUCTION BREAK
CONDITION UNSATISFIED
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 55

	VALID	ADDRESS	MODE
#0			
#1			
:	:	:	:
:	:	:	:
#n			

FIG. 56

	VALID	ADDRESS	DISP	MODE
#0				
#1				
:	:	:	:	:
:	:	:	:	:
#n				

FIG. 57

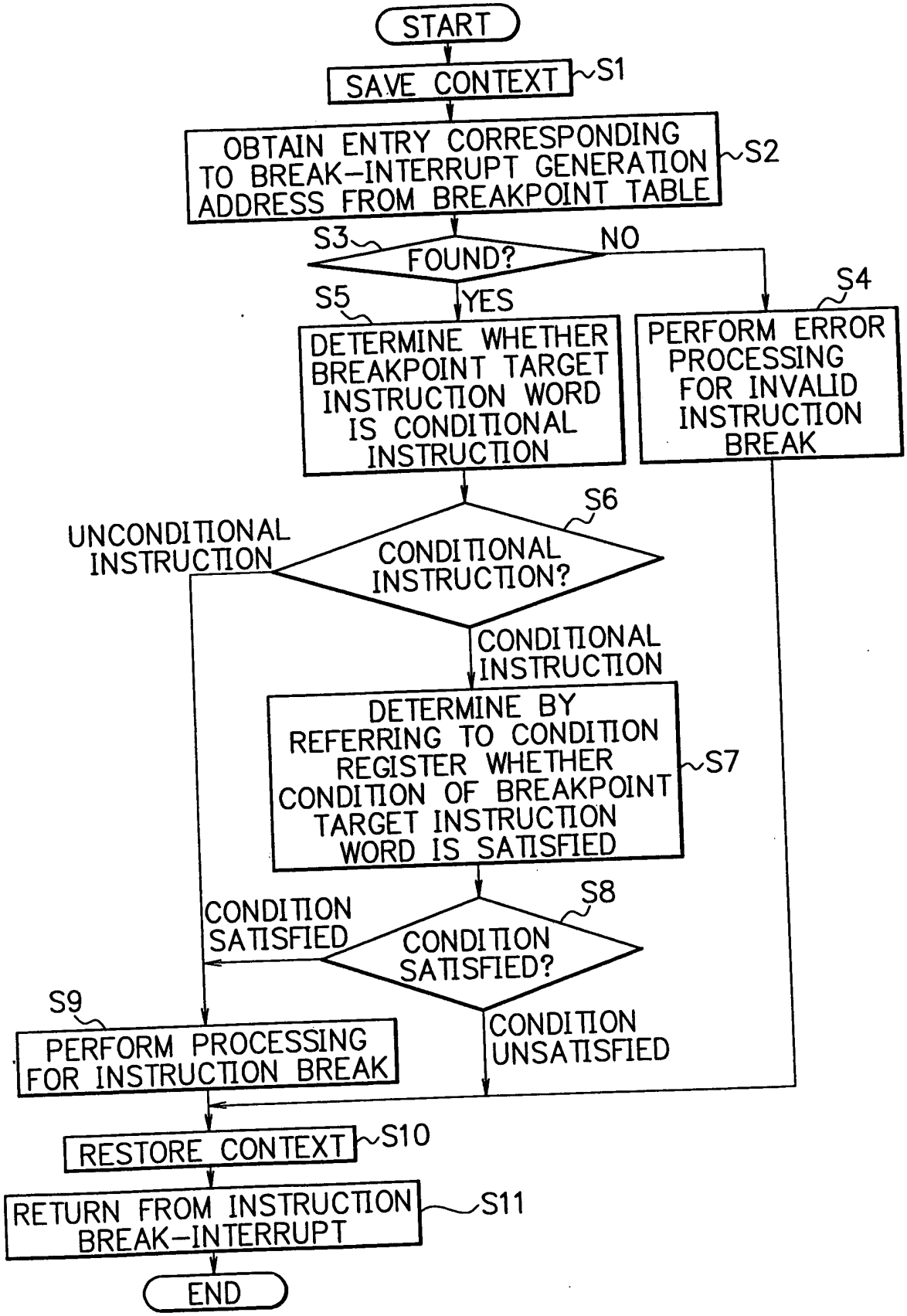

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
YES
S4
S5
DETERMINE WHETHER BREAKPOINT TARGET INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
S6
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION?
CONDITIONAL INSTRUCTION
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
S7
S8
CONDITION SATISFIED
CONDITION SATISFIED?
S9
CONDITION UNSATISFIED
PERFORM PROCESSING FOR INSTRUCTION BREAK
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 58

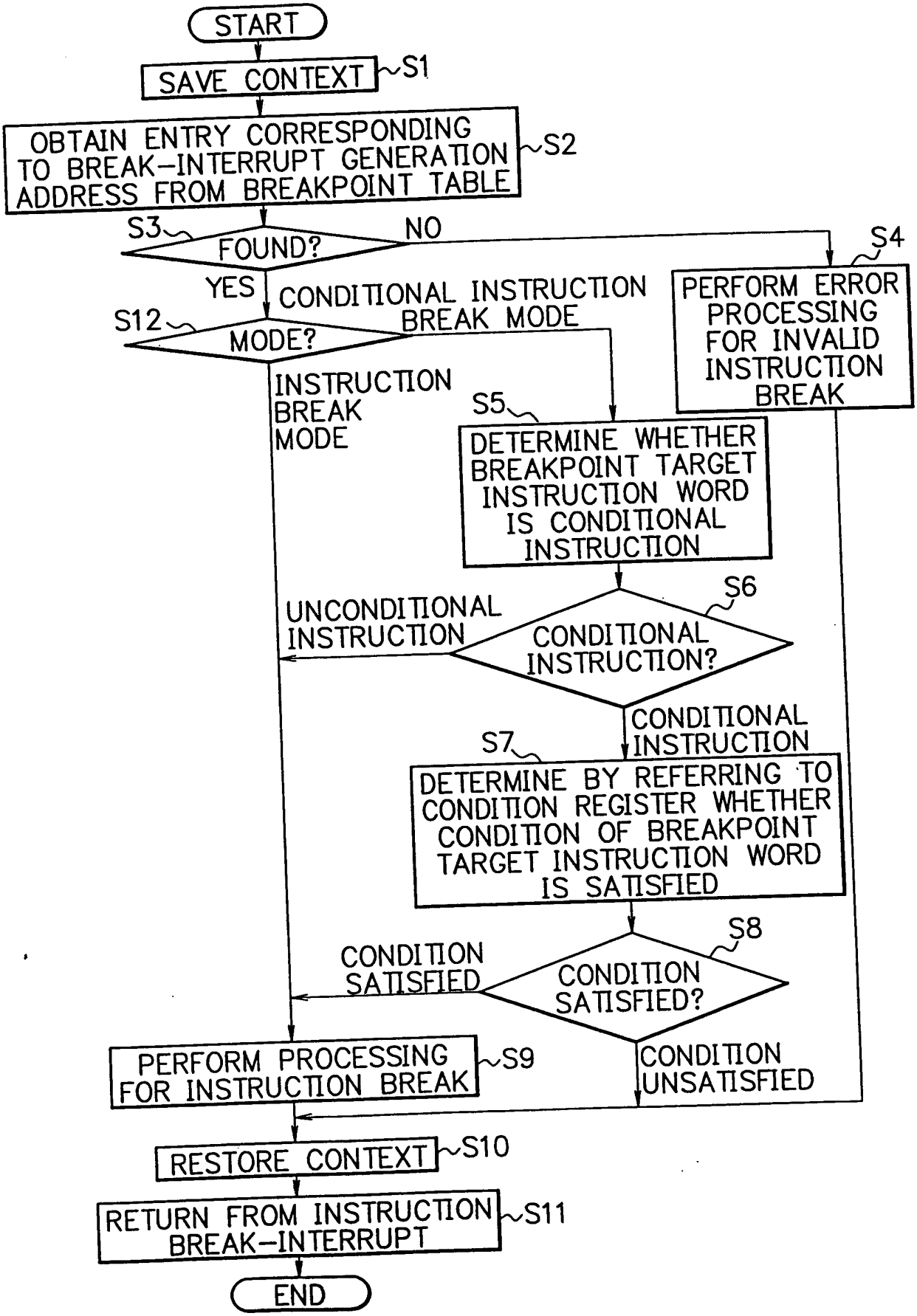

START
SAVE CONTEXT
S1
OBTAIN ENTRY CORRESPONDING TO BREAK-INTERRUPT GENERATION ADDRESS FROM BREAKPOINT TABLE
S2
S3
FOUND?
NO
S4
PERFORM ERROR PROCESSING FOR INVALID INSTRUCTION BREAK
YES
CONDITIONAL INSTRUCTION BREAK MODE
S12
MODE?
INSTRUCTION BREAK MODE
S5
DETERMINE WHETHER BREAKPOINT TARGET INSTRUCTION WORD IS CONDITIONAL INSTRUCTION
S6
UNCONDITIONAL INSTRUCTION
CONDITIONAL INSTRUCTION?
CONDITIONAL INSTRUCTION
S7
DETERMINE BY REFERRING TO CONDITION REGISTER WHETHER CONDITION OF BREAKPOINT TARGET INSTRUCTION WORD IS SATISFIED
S8
CONDITION SATISFIED
CONDITION SATISFIED?
CONDITION UNSATISFIED
PERFORM PROCESSING FOR INSTRUCTION BREAK
S9
RESTORE CONTEXT
S10
RETURN FROM INSTRUCTION BREAK-INTERRUPT
S11
END

FIG. 59

	VALID	ADDRESS	DISP	INSTRUCTION
#0				
#1				
:	:	:	:	:
:	:	:	:	:
#n				

FIG. 60

	VALID	ADDRESS	MODE	INSTRUCTION
#0				
#1				
:	:	:	:	:
:	:	:	:	:
#n				

FIG. 61

	VALID	ADDRESS	DISP	MODE	INSTRUCTION
#0					
#1					
:	:	:	:	:	:
:	:	:	:	:	:
#n					